Design of a QPSK Transceiver for use in Satellite Communication.

by

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Thesis presented in partial fulfilment of the requirements for the degree

Master of Science in Engineering

at Stellenbosch University

Supervisor: Dr. R. Wolhuter

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Abstract

Design of a QPSK Transceiver for use in Satellite Communication.

TA. Verschaeve

Thesis: MEng (E and E)

December 2015

Modern satellites have a wide range of transceivers and communication links, varying entirely with the overall function and mission of the satellite. All satellites however, no matter how small or trivial the mission, have some form of Telemetry, Tracking, and Command (TT&C) requirement. This communication link is critical for the success of the satellite mission, thus it's implementation is traditionally highly robust but slow. Under critical circumstances however, having a high speed TT&C link could potentially shorten and simplify data transfer times during relatively short overflight times of LEO satellites. It can also be the differentiating factor between recovering from a unexpected fault and losing all communication and thus losing the satellite.

In an attempt to address this issue, this project analyzed the difficulties experienced with a traditional TT&C link and used these findings to implement a higher speed TT&C link. To this end simulation software was designed to fully understand the dynamic operation circumstances of LEO satellites. Two S-Band QPSK transceivers were designed and built. The completed transceivers were integrated with an accompanying project, and the overall system performance was tested and evaluated.

Uittreksel

Ontwerp van 'n QPSK Sender / Ontvanger vir gebruik in Satelliet Kommunikasie

TA. Verschaeve

Tesis: MIng (E en E)

Desember 2015

Moderne satellitete het 'n verskeidenheid ontvanger / senders en kommunikasiekanale, wat heeltemal afhanklik is van die funksie en missie van die satelliet. Een eienskap wat wel gedeel word deur alle satelliete, onafhanklik van die grootte of kompleksiteit van die missie, is die noodsaak van Telemetrie, Opsporing en Beheer (TO&B) fasiliteite. Hierdie kommunikasiekanaal is krities vir die sukses van die satellietmissie, dus is die implementasie tradisioneel robuust maar stadig. Onder kritiese omstandighede kan 'n hoër spoed TO&B kanaal die tydsduur en kompleksiteit van data transmissie en ontvangs verlaag vir die relatiewe kort oorvlugtye beskikbaar vir tipiese LEO baaneienskappe. Hierdie hoër spoed TO&B kanaal kan ook die verskil beteken tussen die suksesvolle herstel van 'n foutiewe satelliet en alle kommunikasie verloor, en dus die satelliet verloor.

Om hierdie probleem te probeer adreseer, is daar in hierdie projek analise gedoen om te bepaal wat die probleme is wat ervaar word met tradisionele TO&B implementasies. Wat geleer is uit die analise is daarna gebruik om 'n hoër spoed TO&B kanaal te implementeer. Om hierdie te bereik is daar simulasie sagteware geskryf om die dinamiese werksomgewing van LEO satelliete te verstaan. Twee S-Band QPSK ontvanger / senders is ontwerp en gebou. Hierdie ontvanger / senders is toe geintregreer met 'n mede projek en die totale stelsel is getoets en geevalueer.

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Nomenclature

Constants

$\pi =$	$3.141\,592\,654$	
e $=$	$2.718\,281\,828$	
$k =$	$1.3806488 \times 10^{-23}$	$[\mathrm{m^2\ kg\ s^{-2}\ K^{-1}}]$

Variables

Re_{D}	Reynolds number (diameter)	[ ]
x	Coordinate	[m]
$\ddot{x}$	Acceleration	$[\mathrm{m/s^2}]$
θ	Rotation angle	[rad]
τ	Moment	[N·m]

Vectors and Tensors

$\overrightarrow{\boldsymbol{v}}$	Physical vector

Subscripts

a	Adiabatic
a	Coordinate

Abbreviations

AGC	Automatic Gain Control
VGA	Variable Gain Amplifier
DAC	Digital to Analogue Converter
ADC	Analogue to Digital Converter
GND	Ground
PCB	Printed Circuit Board
IF	Intermediate Frequency
HF	High Frequency
LO	Local Oscillator

TT&C Telemetry, Tracking and Command
SOT-89 Small Outline Transistor, type 89
TSSOP Thin Small Outline Package
SMD Surface Mounted Device
SPI Serial Peripheral Interface
QPSK Quadrature Phase Shift Keying
BPSK Binary Phase Shift Keying
SDR Software Defined Radio
VSWR Voltage Standing Wave Ratio

Chapter 1

Introduction

1.1 Background

Modern satellites have a wide range of transceivers and communication links, entirely dependent on the overall function and mission of the satellite. All satellites however, no matter how small or trivial the mission, have some form of Telemetry, tracking, and command (TT&C). This communication link is used for a wide range of mission critical functions, such as : Software management and upgrades, telemetry and tracking, payload scheduling, movement and positioning, power management. The typical layout and frequency use of this TT&C link uses a VHF up-link and a UHF down-link, with a channel bandwidth of 25kHz. These relatively low frequencies and narrow bandwidth rarely give data rates higher than 9600 bits per second.

Satellites also find themselves in a very dynamic working environment. The operation, orbit, and even the weight changes over the lifetime of the satellite. Inertia wheel friction co-efficients change with extended use, satellite weight changes when fuel is burnt, power storage and solar panel efficiencies change. This environment means that software management and software updates are certain to happen. Sometimes due to accidents or failures, these updates need to happen as soon as possible. This was the case with SumbandilaSat, where an urgent software update was required to correct for a failing inertia wheel. Quite a lot of planning had to go into the update of software of a failing LEO satellite, over a very slow TT&C communication link, in the eight minutes of visibility during a pass.

The scenario described is of course an extreme case, but increasing the speed of the TT&C link while keeping the same level of reliability, would ease this part of operation and could potentially save the overall mission of the satellite.

This increase in speed could be achieved by moving the TT&C link to S band, or any other band allowing higher speed. Due to the method used to do frequency allocation, the bandwidth available per carrier frequency in the S band is far wider than at UHF bands.

1.2 Objectives

It will be attempted to create a TT&C link, which will operate at the same level of reliability, at a higher bandwidth than traditional satellite TT&C links. In achieving this, the following would be required:

- Conduct an in depth study of satellite orbital mechanics and analytically determine the performance of a communication link used by a LEO satellite
- Realize this communication link in the form of simulation software, determine link variance due to orbital mechanics
- Use the simulation results as the limits for the planned TT&C link
- Design two laboratory grade transceivers that operate at a higher bandwidth
- Construct and test individual components of the transceivers.
- Integrate the completed transceivers with a communication back end, created in another Masters project.
- Test and characterize the complete system with analysis of performance

1.3 Summary of Results

The following results were achieved in the completion of this project:

- An in depth study in LEO satellite orbital mechanics was conducted and the associated effect on the particular type of communication link investigated
- A LEO satellite simulation software package, which should be a very useful tool in the link analysis process for future similar work.
- Integrated two S band transceivers with the back end hardware and software created in another Masters project.

- The completed system was tested with the help of HvW, in operational mode. This revealed some non-ideal behavior, which is not unusual and at least provided a clear indication of problems requiring attention in a next iteration.

- It was attempted to carefully analyse the the problem areas observed, in order to assist with successful future elimination.

This project delivered the first version of a high speed satellite TT&C link. The design van be refined,re-designed and adapted from this point forward. The created simulation software package can be used to support the refinement process.

1.4 Outline of Thesis

The layout of this document is as follows:
Chapter 2 starts by giving a basic overview of orbital satellite mechanics and the relevant describing parameters. Focus is then moved over to the conversion techniques required to create a time based simulation of the previously described satellite orbit, as well as simulating the transceiver communication link and effective data rates.
In **Chapter 3**, we take a brief look at the overall research proposed methodology of both the simulation software package and the QPSK transceiver.
Then, in **Chapter 4**, the design process regarding the satellite communication simulator is described, with results of the simulation software package shown at the end of this chapter.
Using a range of the results generated by these simulations, the QPSK transceiver design is covered in **Chapter 5**. Individual component performance is evaluated at the end of this chapter. In **Chapter 6** we then analyze the overall system performance
Finally, in **Chapter 7**, we draw conclusions around the results observed and recommend future work on the topic.

Chapter 2

Literature Review

2.1 Introduction

This chapter summarizes the research done to build the proposed satellite communication simulator and the QPSK transceiver. The primary focus is on satellite orbital mechanics and the techniques associated with satellite communication.

2.2 Satellite Orbital Mechanics

There are several methods to represent a satellite orbit. The method chosen was an implementation of Kepler's basic three rules concerning elliptical orbit [9, chapter 2, page 27].

2.2.1 Satellite orbits and Kepler's Rules

It is important to note that this method does not take into account the effect of gravitational height decay or the possible drag created by the atmosphere. For the short term simulations that this project would generate, long term effects like these could be ignored.

Kepler's first law states that a satellite with a closed orbital path will travel around the earth in elliptical paths with the center of the earth located at one of the elliptical focus points .

$$e = \sqrt{1 - \frac{b^2}{a^2}} \tag{2.2.1}$$

The eccentricity (e) describes the shape of an ellipse

$$r = \frac{a(1 - e^2)}{1 + e(\cos v)} \tag{2.2.2}$$

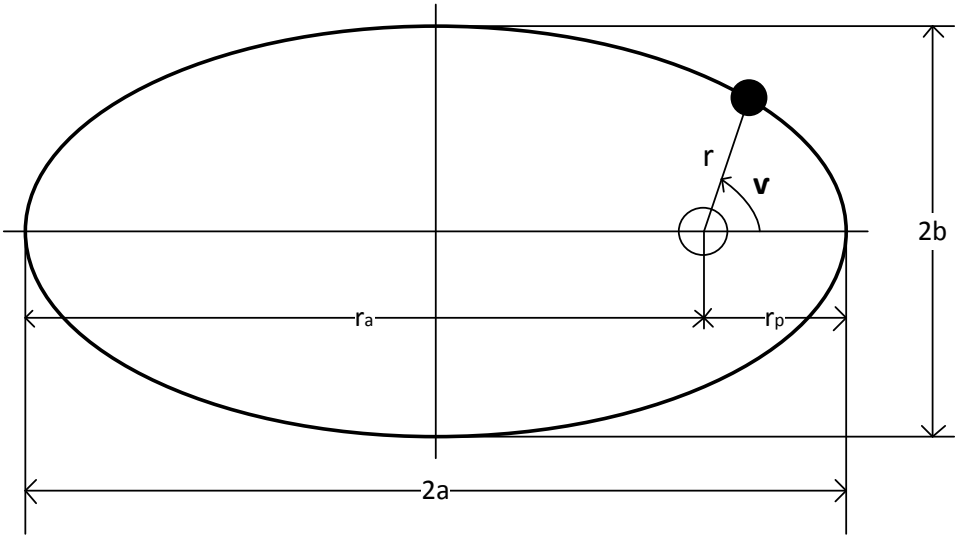

Figure 2.1: The ellipse and the parameters used to define it (v_r)

The distance between the earth and the satellite (r) varies as the true anomaly (v) angle changes

$$T^2 = \left(\frac{4\pi^2}{\mu}\right) a^3 \tag{2.2.3}$$

In his third law, Kepler proves that the orbital period (T) of a satellite is determined by the semi-major axis (a) of the orbit with μ being the gravitational parameter for earth (3.986 x 10^5 km^3/sec^2) Thus with these equations and the parameters describing the orbit of a satellite, the distance from the focus point (the center of the earth) can be calculated for any angle v.

Using Newton's laws of angular momentum and total energy, it can be proven that the velocity of a satellite equals :

$$v = \sqrt{2\mu\left(\frac{1}{r} - \frac{1}{2a}\right)} \tag{2.2.4}$$

As seen above in equation 2.2.4 the velocity of a satellite is determined by the semi major axis a, the gravitational parameter of the body around which it's orbiting, μ, and the distance r orbiting around which the body is orbiting. The instantaneous position and velocity of a satellite can now be calculated for the angle of rotation v. This position can of course be converted into Cartesian coordinates using basic trigonometry.

2.2.2 Satellite Swath Width

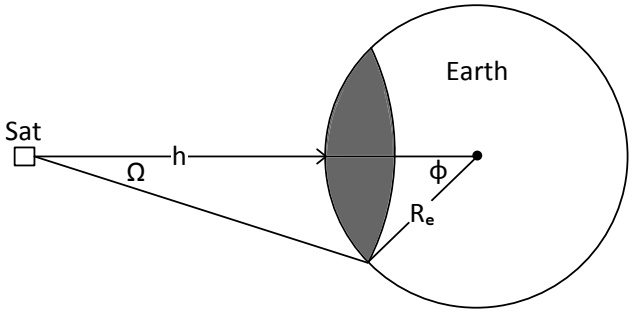

Figure 2.2: Two discrete steps in the orbit of a satellite

The amount of earth visible to a satellite at any time is a function of the height above the planet [9, chapter 2, page 39] . As shown as the grey area in figure 2.2. This area can be calculated as:

$$A = 2\pi {R_e}^2 \sin\phi \tag{2.2.5}$$

With ϕ as:

$$\phi = \cos^{-1}\left(\frac{R_e}{R_e + h}\right) \tag{2.2.6}$$

and Ω as:

$$\Omega = \sin^{-1}\left(\frac{R_e}{R_e + h}\right) \tag{2.2.7}$$

Another parameter that could be of interest is the swath width of the satellite, which is the distance from one tangential horizon to the other. Swath width is denoted as SW.

$$SW = 2R_e\phi \tag{2.2.8}$$

2.2.3 Orbit Description Standard : TLE

There are several ways to represent the orbital parameters of a satellite. The most widely used is a system developed by the North American Aerospace Defense Command (NORAD) called the TLE or Two Line elements of a satellite. This is a structured format used to transmit the Keplerian elements of a satellite.

Shown below as an example is the TLE of the international space station (ISS). The package contains various data concerning the satellite such as Launch date , classification, etc.

1 25544U 98067A 11194.88111111 .00008767 00000-0 11284-3 0 7072
2 25544 51.6409 26.3035 0010794 321.9521 241.0016 15.59878357725073

For the purpose of the work done here, we are only interested in three of the TLE parameters, which are:

- The Orbital inclination - 2nd line, 3rd element
- The Orbit eccentricity - 2nd line, 5th element
- The Satellite mean motion in revolutions per day - 2nd line, 8th element

Using Kepler's rules and these three TLE parameters, we can accurately describe the orbital path of a LEO satellite.

2.2.4 Polar and Cartesian Co-ordinates

The ECEF, or earth centered earth fixed, co-ordinate system is widely used in calculations and representations of the earth. This frame is attached to the earth itself at its center, and allows for use of both Cartesian and polar coordinates, as shown in figure 2.3 [1].

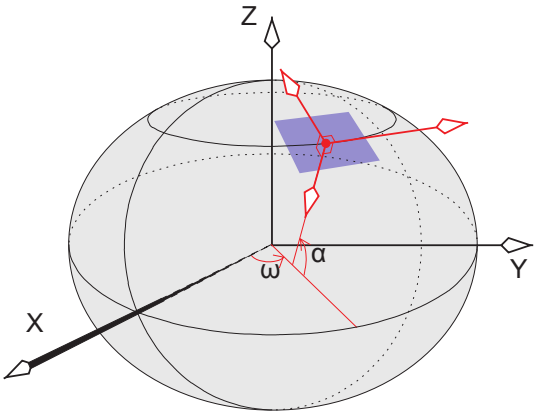

Figure 2.3: The ECEF coordinate system [1]

Elliptical Polar to Cartesian

The conversion of a polar (latitude, longitude and height) coordinate set to Cartesian (X,Y and Z) is described in equations 2.2.9.

$$\begin{aligned} X &= \left(\frac{a}{\sqrt{\cos^2\alpha + \frac{b^2}{a^2}\sin^2\alpha}} + h \right) \cos\alpha\cos\omega \\ Y &= \left(\frac{a}{\sqrt{\cos^2\alpha + \frac{b^2}{a^2}\sin^2\alpha}} + h \right) \cos\alpha\sin\omega \\ Z &= \left(\frac{b}{\sqrt{\frac{a^2}{b^2}\cos^2\alpha + \sin^2\alpha}} + h \right) \sin\alpha \end{aligned} \tag{2.2.9}$$

With the following parameters describing the oblate spheroid that is the earth:

- Semi-major: a = 6 378 137m
- Semi-minor: b = 6 356 752.3142m

A position in terms of latitude and longitude coordinates can be converted to Cartesian coordinates.

Cartesian to Elliptical Polar

The opposite of the conversion shown by equations 2.2.9 could also be of use.

$$\begin{aligned} \omega &= cos^{-1}\left(\frac{X}{\sqrt{X^2+Y^2}} \right) \\ \alpha &= tan^{-1}\left(\frac{a^2}{b^2}\frac{Z}{\sqrt{X^2+Y^2}} \right) \\ h &= \frac{\sqrt{X^2+Y^2}}{cos\alpha} - \frac{a^2}{\sqrt{a^2cos^2\alpha + b^2sin^2\alpha}} \end{aligned} \tag{2.2.10}$$

The equation for α is actually a first estimate in an iterative process, but the first estimate is already accurate to approximately five decimal places,which was found to be sufficient for this application.

2.2.5 Rotation in 3D

In section 2.2.1 we calculated the orbital path of a satellite. In that section we assumed that in the 3D Cartesian described space, the satellite orbits in the

$z = 0$ plain. This is of course not always the case since the inclination angle of satellites vary widely. We now need to rotate the calculated orbital path in three dimensions to allow for the simulation of any satellite orbit inclination.

This rotation can be done by multiplying the satellite position vector (x) with a rotation matrix $(R_n(\theta))$ to yield the new rotated position vector x' [1].

$$x' = R_n(\theta)x \tag{2.2.11}$$

Where $R_n(\theta)$ specifies a right handed rotation with angle θ about an axis aligned with a unit vector n

The rotation matrix can be written in the following way:

$$R_n(\theta) = (1 - cos(\theta))nn^t + cos(\theta)I_3 + sin(\theta)n^\times \tag{2.2.12}$$

With n as the unit vector

$$n = \begin{bmatrix} n1 \\ n2 \\ n3 \end{bmatrix} \tag{2.2.13}$$

n^t as the transpose of n, I_3 as a 3 x 3 identity matrix and $n^\times$ as:

$$n^\times \equiv \begin{bmatrix} 0 & -n_3 & n_2 \\ n_3 & 0 & -n_1 \\ -n_2 & n_1 & 0 \end{bmatrix} \tag{2.2.14}$$

Thus we now have the tools to rotate a Cartesian x, y and z coordinate set around a unit vector n with a angle of θ degrees

2.3 Communication Systems

Now that we know how a LEO satellite revolves around a planet, possibly earth, we need to address the communication aspect and the parameters of it that are unique to satellite communication.

2.3.1 Doppler Frequency Shift

Since LEO satellite communication consists of two points that accelerate and decelerate relatively towards each other, a Doppler shift is observed in the received frequencies of both the satellite and the ground station. We need to fully understand the effect and the extent of frequency change experienced by the receivers[10, 10.5.6.2].

Relative Frequency Shift

The shift in the received frequency due to the movement of the receiver and/or transmitter can be calculated as follows:

$$f = \left(1 - \frac{V_{s,r}}{c}\right) f_o \tag{2.3.1}$$

- f = observed frequency
- c = speed of light
- $V_{s,r}$ = relative speed between source and receiver

This equation uses the relative velocity, $V_{s,r}$, experienced between the source and the receiver.

Relative Velocities

In the previous section we've shown that we require the satellite and ground station relative velocities to calculate the effect the Doppler shift would have on the transmitted signal. To calculate these velocities we start with the movement vectors. To avoid confusion, we create two vectors, namely : $\bar{V}_{ES}$, which is the velocity of the earth relative to the satellite and $\bar{V}_{SE}$, which is the velocity of the satellite relative to the earth.

The proposed simulation model would create arrays containing the x, y and z co-ordinates of the satellite and the base station (defined as SAT_{xyz} and $EARTH_{xyz}$ below), from which we can calculate the vectors of movement for each time interval. Keeping with the annotation explained above, the velocity vectors $\bar{V}_{SAT}$ and $\bar{V}_{EARTH}$ for time interval 0 can be calculated as :

$$\begin{aligned} \bar{V}_{SAT}(0) &= SAT_{xyz}(1) - SAT_{xyz}(0) \\ \bar{V}_{EARTH}(0) &= EARTH_{xyz}(1) - EARTH_{xyz}(0) \end{aligned} \tag{2.3.2}$$

Using $\bar{V}_{SAT}$ and $\bar{V}_{EARTH}$ we can calculate $V_{s/e}$, the velocity of the satellite in respect to the earth and $V_{e/s}$, the velocity of earth in respect to the satellite.

$$\begin{aligned} \bar{V}_{s/e} &= \bar{V}_{SAT} - \bar{V}_{EARTH} \\ \bar{V}_{e/s} &= \bar{V}_{EARTH} - \bar{V}_{SAT} \end{aligned} \tag{2.3.3}$$

To find the direction between the two points, the unit pointing vectors $\bar{r}_{se}$ and $\bar{r}_{es}$ are calculated for each iteration[11].

$$\begin{aligned} \bar{r}_{se} &= \frac{x_s - x_e}{\|r\|}\mathbf{i} + \frac{y_s - y_e}{\|r\|}\mathbf{j} + \frac{y_s - y_e}{\|r\|}\mathbf{k} \\ \bar{r}_{es} &= \frac{x_e - x_s}{\|r\|}\mathbf{i} + \frac{y_e - y_s}{\|r\|}\mathbf{j} + \frac{y_e - y_s}{\|r\|}\mathbf{k} \\ \|r\| &= \sqrt{(x_s - x_e)^2 + (y_s - y_e)^2 + z_s - z_e)^2} \end{aligned} \tag{2.3.4}$$

Using the respective velocities and the unit pointing vectors calculated above, the relative velocities $\bar{V}_{SE}$ and $\bar{V}_{ES}$ are calculated using the dot product between them

$$\begin{aligned} \bar{V}_{SE} &= \bar{V}_{s/e} \cdot \bar{r}_{se} \\ \bar{V}_{ES} &= \bar{V}_{e/s} \cdot \bar{r}_{es} \end{aligned} \tag{2.3.5}$$

With these relative velocities, we can now calculate the difference in received frequencies due to the experienced Doppler Shift.

2.3.2 Transceiver Performance

The final measurement of a communication channel is the rate at which data can be transmitted and successfully received. The first parameter we're interested in, is the maximum data rate achievable for a certain signal quality. This limit, also know as the Shannon capacity, is explained below.

Channel Capacity

Without taking any form of signal modulation into account, the channel capacity or Shannon capacity, gives us a theoretical maximum data rate achievable, for a channel with a specified bandwidth and signal quality [12].

$$C = B \times log_2\left(1 + \frac{S}{N_o}\right) \tag{2.3.6}$$

With C as the maximum baud rate in bits per second and B as the channel bandwidth available in Hz. S is the received power in watts and N_o is the noise power in watts, calculated later in equation 2.3.18.

Signal to Noise Ratio - SNR

Another method to describe the quality of a communication channel is with its SNR, or signal to noise ratio. This value, often given in dB, can be calculated as :

$$SNR_{dB} = 10 \times log_{10}\left(\frac{\text{Signal Power}}{\text{Noise Power}}\right) = 10 \times log_{10}\left(\frac{P_{avg}}{N_o}\right) \tag{2.3.7}$$

Bit Error Rate - BER

Unfortunately a communication channel will always be prone to errors. For a QPSK modulated signal, the type of modulation proposed for the system, we can calculate the expected amount of errors per second [13]. This is known as the BER , or bit error rate.

$$BER = \frac{1}{2} \text{ erfc } \left(\sqrt{\frac{E_b}{N_o}} \right) \tag{2.3.8}$$

The erfc function used above, known as the complimentary error function, describes the cumulative probability curve of a Gaussian distribution. E_b, given in Joules, or Watts per second, calculated as:

$$E_b = \frac{P_{avg}}{R_b} \tag{2.3.9}$$

With R_b as the baud rate in bits per second and P_{avg} as the average received power in watts, described below in section 2.3.3.

2.3.3 Received Power

To calculate the theoretical received power at the demodulation end of the transceiver, we need to do a power link budget calculation. The basis for the calculation starts with the Friis transmission equation, shown below[10].

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi R} \right)^2 \tag{2.3.10}$$

Where

- P_r - received power in watts
- P_t - transmitted power in watts
- G_t and G_r- respective antenna gains
- R - relative distance between the two antennas
- λ - wavelength of the signal transmitted (in the same units as R)

This equation can be converted into decibels which then simplifies to:

$$P_r = P_t + G_t + G_r + 20 \log_{10} \left(\frac{\lambda}{4\pi R} \right) \tag{2.3.11}$$

The last part of this equation is known as the free space loss (FSL) factor, so equation 2.3.11 simplifies further to

$$P_r = P_t + G_t + G_r - L_{FSL} \tag{2.3.12}$$

With L_{FSL} defined as

$$L_{FSL} = 20 \log_{10} \left(\frac{4\pi R}{\lambda} \right) \tag{2.3.13}$$

Equation 2.3.12 forms the basis of our link budget calculation. We will expand this by adding further gain and loss factors specific to the transceiver layout.

Average Signal Power

For many of the calculations and measurements done, we require a representation of average signal power in terms of the peak to peak voltage. For this representation, we start with the standard power equation:

$$P_{avg} = \frac{V^2}{R} \tag{2.3.14}$$

We now substitute the voltage with a sinusoidal signal, V = $Asin(\omega t)$, which generates the following equation:

$$P_{avg} = \frac{A^2 sin^2 (\omega t)}{R} \tag{2.3.15}$$

We can now substitute the sin squared factor with:

$$sin^2 (\omega t) = \left(\frac{1 - cos (2\omega t)}{2} \right) \tag{2.3.16}$$

And since we know that the average of $cos (2\omega t)$ is 0, the average power can be written as :

$$P_{avg} = \frac{A^2}{2R} \tag{2.3.17}$$

2.3.4 Signal Chain Loss Factors

To calculate the overall received power, we need to expand on the Friis Transmission equation above. (equation 2.3.12)
Any component that adds gain to the signal chain is rather self explanatory. There are however, many different loss factors that need to be taken into account. Some of these are explained below.

Conversion Loss

Ideally a mixer would have perfect impedance matching at all three ports, which is rarely the case considering a different frequency at the LO (local osccilator), IF (intermediate frequency) and RF (radio frequency). This impedance mismatch coupled with the generation of unwanted mixing harmonics and resistive losses make up a mixers conversion loss. This loss applies for both up and down mixing and is normally in the order of 4-7 dB in the 1-10 GHz range. [14, sec. 7.1]

Cable and Connector Loss

Any point of connectivity between two components in a transceiver experiences loss due to the method used to connect the two. This loss is attributed to connector and cable impedance values. Additional loss could be present due to a mismatch in these impedance values and the system impedance. For this specific project, all IF and RF subsystems are connected by RG-174 co-axial cable and SMA connectors. The RG-174 has an approximate loss of 139.48 dB per 100 m at 2.3GHz (The maximum frequency used in the system) and a connector loss of approximately 0.5dB per connector. The average value of L_{con} using the specified cable and connector was usually in the order of 1.4 - 2dB.

Attenuation Due to Atmospheric Conditions

Rain and fog have two effects on the transmitted signal which are : Attenuation and cross polarisation. These effects need to be identified and there impact on the proposed communication system analysed.

Cross Polarisation

Rain can cause a energy transfer from one polarisation to an orthogonal polarisation due to differential attenuation. These effects were deemed negligible for the operating frequencies chosen. This is due to the size of rain drops and other atmospheric precipitation (ice clouds , fog) versus the wavelength of proposed communication. The effects of cross polarisation only become measurable at frequencies of 4GHz and higher [10].

Rain Attenuation

Rain attenuation in communication is given as:

$$A_{RAIN} = \gamma_R L_e$$

With L_e as the effective signal path in km and γ_R as the specific attenuation (dB/km) and is effected by the following:

- Communication frequency
- Base station location (latitude and height above sea level)
- Rain intensity

The calculation of γ_R is a relatively complex process but could easily be done in Matlab®. The effects were negligible for any frequencies under 10 GHz, thus taking it into account when calculating the received power would have no merit [10].

2.3.5 Receiver Noise

We now have all the parameters to calculate the received power parameter required in the data rate equations shown in section 2.3.2. We now need to focus on the receiver noise.

Noise Power

The noise power present at the output of a receiver, N_o, can be calculated as:

$$N_o = kT_{sys}BG_{rec} \tag{2.3.18}$$

Where k is the Boltzmann constant, B is the channel bandwidth, T_{sys} is the system noise temperature and G_{rec} is the receiver gain [15].

System Noise Temperature

The system noise temperature used to calculate the noise power in equation 2.3.18 is a combination of the two noise sources at the input of the receiver, as shown below in figure 2.4.

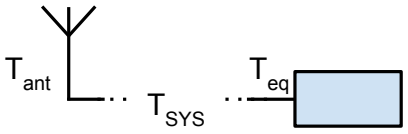

Figure 2.4: Factors that influence the system noise temperature, T_{sys}

Thus we define this combination of antenna noise temperature T_{ant} and effective noise temperature T_{eq} as system noise T_{sys}. Mathematically this relationship is :

$$T_{sys} = T_{eq} + T_{ant} \tag{2.3.19}$$

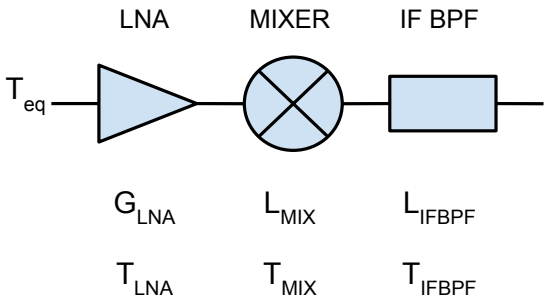

Figure 2.5: Receiver layout example with noise temperatures and gains

Effective Input Noise Temperature

This noise temperature value is a culmination of all noise temperatures present in the receiver chain. Shown below in figure 2.5 is an example of a receiver chain, from which we can calculate T_{eq}, the effective input noise temperature[10, 5.2.2.3].

With the noise temperatures and gains shown in figure 2.5, this effective input noise temperature is written as:

$$T_{eq} = T_{LNA} + \frac{T_{MIX}}{G_{LNA}} + \frac{T_{IF}}{G_{LNA}G_{MIX}} \tag{2.3.20}$$

Component Noise Figure

The term noise figure (NF) of a component or network is the ratio of SNR experienced at the input of the network vs the SNR experienced at the output of the network. Thus a NF is a indicator of the extent of how much a component or network degrades the quality of the signal that passes through it. NF is used by component manufacturers, to describe the effect the component in question would have on a system. The conversion between NF (in dB) and effective temperature, T_{comp} in K, is done as follows[16]:

$$T_{comp} = T_{REF} \times \left(10^{\frac{NF}{10}} - 1\right) \tag{2.3.21}$$

With $T_{REF} = 290$K unless otherwise specified

With this equation, we can calculate a specific components noise temperature, for a impedance matched system.

Base Station Antenna Noise Temperature

The base station antenna noise temperature consists of two noise sources. Noise due to ground radiation (T_{GROUND} and noise due to the sky (T_{SKY}).

T_{SKY} can be determined using the angle of elevation (longitude) of the antenna and operating frequency. This relationship is only available in measured results and is non-linear. Thus a worst case scenario of 0° is taken, which equates to a T_{SKY} value of 80K [10, fig 2.16].

This temperature varies between clear skies and rainy conditions. The clouds and rain act as an attenuator to the noise temperature, not just the signal power as described in section 2.3.4. But much as the attenuation described in that section, it's effect on noise temperature is negligible for the frequencies discussed here.

T_{GROUND} is due to radiation from the earth that is captured by the side lobes of the antenna[10, chapter 5]. The contribution of each lobe can be described as:

$$T_i = G_i(\Omega_i/4\pi)T_G \tag{2.3.22}$$

With G_i as the gain of the lobe at angle Ω_i and T_G as the brightness temperature of the ground. The relationship between T_G vs elevation angle is measured and non-linear, but we can assume the following:

$T_G = 290K$ for lobes with an elevation angle less that -10°
$T_G = 150K$ for lobes with an elevation angle between -10° and 0°
$T_G = 50K$ for lobes with an elevation angle between 0° and 10°
$T_G = 10K$ for lobes with an elevation angle between 10° and 90°

Thus by calculating the ground radiation each side lobe of the antenna absorbs, we can calculate the total G_{GROUND}. The total antenna temperature is described as

$$T_A = T_{SKY} + T_{GROUND} \tag{2.3.23}$$

Satellite Antenna Noise Temperature

Since we are assuming that the satellite antenna will have a narrow antenna beam width, it's antenna noise temperature would only be due to the radiation generated by the earth. This noise temperature depends on the orbital position of the satellite and the frequency used for communication. This relationship in terms of satellite longitude and frequency is measured and non-linear. Thus for these purposes the worst case scenario longitude as 30° East is taken, which gives an antenna noise temperature of 185K.

2.3.6 Effect and Analysis of an Unmatched Component

Standard signal power and noise analysis techniques rely on the fact that all components are perfectly matched at a specified impedance. In real world applications however, this is frequently not the case. Especially with non-linear components such as amplifiers and mixers. A impedance mismatch between

two components generates a non-ideal Voltage Standing Wave Ratio (VSWR). This deviation from ideal VSWR (not 1:1), has a detrimental effect on the noise figure of the component as well as the component gain or loss factor.

To quantify the exact effect that an impedance mismatch can have on the performance of a component, we need to look at the parameters affected. Shown below in figure 2.6 is a passive two port network representation of a component in a system. With the input or generator connected to port **1** and the output or load connected to port **2**. This network is characterized by its S-parameter matrix **[S]** and and experiences the following reflection coefficients:

- Γ_s is the reflection coefficient towards the generator
- Γ_L is the reflection coefficient looking towards the load
- Γ_{in} is the reflection coefficient looking towards the input of the network, port **1**
- Γ_{out} is the reflection coefficient looking towards the out of the network, port **2**

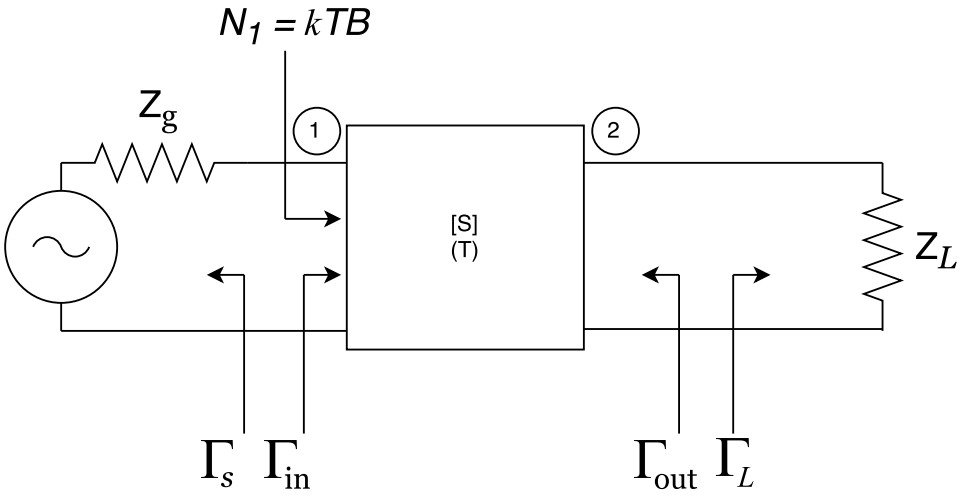

Figure 2.6: Description of a Two Port Network and it's Relevant Parameters [2, fig 10.25]

With this standard model, we can now calculate how this mismatch affects the gain and noise of the component.

Effect on Component Noise Figure

The noise at the output of the network, N_2, can be written as[2, eq 10.24]:

$$N_2 = G_{21}kTB + G_{21}N_{add} \tag{2.3.24}$$

With k is the Boltzmann constant, B is the channel bandwidth, T as noise temperature and N_{add} as the noise generated internally by the network. The final term, G_{21}, which is the power available from the network divided by the power available form the source.

Given the input noise as kTB and the network being at the same temperature as the input noise temperature T, we know that the output noise power must be $N_2 = kTB$. Thus we cal solve for N_{add} in equation 2.3.24 as :

$$N_{add} = \frac{1 - G_{21}}{G_{21}}kTB \tag{2.3.25}$$

From which we can write the equivalent noise temperature T_e as:

$$T_{eq} = \frac{N_{add}}{kB} = \frac{1 - G_{21}}{G_{21}}T \tag{2.3.26}$$

and we can specify the component noise figure as :

$$F = 1 + \frac{T_{eq}}{T_0} = 1 + \frac{1 - G_{21}}{G_{21}}\frac{T}{T_0} \tag{2.3.27}$$

In a lengthy process, not seen as relevant for the purpose of this research, it can be shown that the network forward gain factor, G_{21}, is equal to[2, eq 10.25]:

$$G_{21} = \frac{|S_{21}|^2(1 - |\Gamma|^2)}{|1 - S_{11}\Gamma_s|^2(1 - |\Gamma_{out}|^2)} \tag{2.3.28}$$

Thus by substituting the equation for the available power gain, G_{21} into the noise temperature equation 2.3.27, we get the following:

$$T_{eq} = \frac{(L - 1)(L + |\Gamma_S|^2)}{L(1 - |\Gamma_S|^2)}T \tag{2.3.29}$$

This equation for T_{eq} describes the noise temperature of a component relative to the reflection and losses that are caused by impedance mismatch.

Effect on Component Gain

The next aspect effected by the impedance mismatch is the gain / loss of a the component. This mismatch can occur at both the input and output ports of the component Thus along with the inherent loss or gain of a component, an impedance mismatch can add two additional possible loss factors. They are:

- Input impedance mismatch loss - $L_{in-mismatch}$
- Output impedance mismatch loss - $L_{out-mismatch}$

To calculate these values, we must first calculate the reflection coefficient experienced. If the impedance of bot h components are known, the reflection co-efficient can be calculated as:

$$\Gamma = \frac{Z_L - Z_O}{Z_L + Z_O} \tag{2.3.30}$$

If the voltage standing wave ratio (VSWR) at the input of the component is known, the reflection co-efficient can be calculated as:

$$\Gamma = \frac{VSWR - 1}{VSWR + 1} \tag{2.3.31}$$

With this reflection co-efficient value, the loss due to impedance mismatch in dB can be calculated as[2, eq14.28]:

$$L = -10\log(1 - |\Gamma|^2) \tag{2.3.32}$$

Depending on what values you have available (VSWR or impedances), the reflection coefficient at a port can be calculated. With this reflection coefficient and equation 2.3.32, one can calculate the additional loss a component would experience due to impedance mismatch.

2.3.7 Frequency Allocations

The system would need to operate within ICASA standards in all manners, this included frequency usage. The ICASA Project SABRE (South African Band Re-planning Exercise) documentation was used as a reference for frequency allocation. The Sabre 1 report addressed frequencies from 20MHz to 3GHz. According to this report for frequencies ranging from 1920-2300MHz:
note 3.10.11 : 2025 - 2110 and 2200 - 2290 MHz

- "Channel arrangements for the use of this band for fixed services are described in both ITU-R Recommendation F.1098 and CEPT Recommendation T/R 13-01."
- "These recommendations describe a channel plan in which the band is divided into dual frequency channels with carrier spacing 14 MHz and Tx/Rx separation 175 MHz."
- "Carrier spacings of 7, 3.5 and 1.75 MHz are also possible by means of channel subdivision."

Let f_0 be the center frequency of the band, which equals 2 155 MHz
f_n be the center frequency of one channel in the lower half of this band
f_n' be the center frequency of one channel in the upper half of this band

The ITU-R Recommendation F.1098 gives the following description:
The frequency usage can then be described as :

$$f_n = f_0 - 136.5 + 14n$$
$$f_n' = f_0 + 38.5 + 14n$$

where: $n = 1, 2, 3, 4, 5$ or 6.

Taking these regulations into account the system would operate using the following HF frequencies:

Table 2.1: HF Frequency Usage

Channel	Centre Frequency (MHz)	Bandwidth (MHz)
Uplink	2032.5	1.75
Downlink	2207.5	1.75

ICASA also would allow channel spacings of 14, 7 and 3.5MHz. All hardware would support these higher bandwidths, except the filters chosen. With the baseband hardware proposed by Hendrik Van Wyk, 1.75MHz of bandwidth per channel was found to be adequate.

2.3.8 Modulation Scheme and System Layout

For ease of use and ease of analysis, BPSK was selected as the modulation scheme. However, during the component research and acquisition phase of the project, a QPSK modulator was selected as a optimal replacement. Using QPSK modulation / demodulation allowed for pure BPSK operation as originally intended, but added the flexibility of experimenting with M-ary quadrature modulation

A superhetrodyne transceiver layout was selected. This approach uses a intermediate frequency when mixing between the modulated baseband signal and the transmission frequency. This intermediate frequency approach would simplify the modulator / demodulator design, ease the strict requirements on component selection and any Doppler shift frequency detection could be done at a relatively low frequency, simplifying it's design and operation.

This selection of this intermediate frequency would completely depend on component selection and availability.

2.3.9 Antenna Types

The simulation software and transceiver design proposed for this project would require antennas for transmitting and receiving. Four antenna types were analyzed, namely : Quadrifilar helix , patch, Yagi Uda and the parabolic dish. The actual operation of these antennas were not within the scope of this project, but we'd need to understand several of the antenna parameters for implementation. We required the relationship between antenna size parameters and the radiation pattern (EIRP). The EIRP of two of the antennas were stored in the form of lookup tables, these were : Quad Helix and Yagi. The EIRP of the other two antennas were calculated in the software. The equations for the parabolic dish gain and beam width were easier to calculate than to store. (This also added the flexibility of trying different dish sizes with the same simulation parameters) The same is true for the patch antenna.

Quadrifilar Helix Antenna

The Quad Helix antenna is widely used in satellite communications , since there can be no polarization angle mismatch between the transmitter and receiver. To use the EIRP of the antenna in the simulation software, the gain vs angle values of an existing antenna were taken and put into a lookup table.

Yagi Uda Antenna

The Yagi antenna is a favorite since it is robust and easy to construct. As with the quad helix, the gain vs angle values of a three element yagi were stored in a lookup table.

Patch Antenna

Easy to design for operation at an exact required frequency, and easy to manufacture. This robust antenna design is rather complex, but for the purpose of this project we're only interested in the effective radiation pattern of a patch antenna, seen below in equation 2.3.33 [17, chapter 17.6].

Notmalized gain is given as :

$$g(\theta,\phi) = \left(cos^2\theta cos^2\phi + cos^2\phi\right)\left|F(\theta,\phi)\right|^2 \tag{2.3.33}$$

Where $F(\theta,\phi)$, the normalized radiation vector, can be described as :

$$F(\theta,\phi) = cos\left(\pi l sin\theta cos\phi\right)\frac{sin\left(\pi w sin\theta sin\phi\right)}{\pi w sin\theta sin\phi} \tag{2.3.34}$$

With l as the patch length and w as the patch width. By adding the maximum directional gain to the normalized gain g shown above, we have an equation for antenna gain vs angle for a patch antenna with a certain size.

Parabolic Dish Antenna

The narrow beam width but high gain of the parabolic dish makes it optimal for high data rate applications. Since this beam width is so narrow, it was decided to calculate the 3 dB cutoff of the antenna and it's maximum gain. The maximum gain was used in link budget calculations, whenever the field of view was within the 3 dB cut off beam width of the antenna. The maximum gain in dB, g_{max} is calculated as[17, chapter 17.7]:

$$g_{max} = 10log\left(n\frac{\pi D}{\lambda}\right)^2 \tag{2.3.35}$$

Where D is the diameter of the dish in meter ,n is the efficiency factor and λ is wavelength in meter, which can be calculated as :

$$\lambda = \frac{c}{f} \tag{2.3.36}$$

With c as the speed of light in meters per second and f as the signal frequency in hertz.

With this information we can also estimate the beam width ψ, also known as the 3dB cutoff angle, using the following equation :

$$\psi = \frac{70\lambda}{D} \tag{2.3.37}$$

2.4 Brief Summary and Prognosis for Next Chapter

With the basic orbital mechanics defined by Kepler's rules, a single pass of a satellite could be calculated in 2D. Using the co-ordinate conversions and rotation in 3D, a time based 3D simulation of a satellite orbiting the earth could be generated. This satellite path simulation could generate distances, angles and speeds of the satellite and the ground station. Using these ground station and satellite parameters we can calculate the Doppler shift that will affect the transmitted signal.

We also described the following communication channel analysis methods and parameters:

- The absolute maximum baud rate possible on a communication channel can be calculated by equation 2.3.6, know as the channels Shannon capacity
- The Shannon capacity and other communication measurement parameters use the SNR, which is a ratio of the received signal power vs the received noise power.

- The received signal power, P_{avg} is calculated using the Friis transmission equation.
- This received signal power can also be expressed as energy per bit, or E_b.
- The received noise power, N_o, is effected by the system bandwidth, system gain and the system noise temperature.
- The final test of a communication link is to observe the amount of errors that occur during data transfer. This rate is known as a channels BER, or bit error rate.

In the next chapter, the learnings around satellite orbital mechanics and communication system performance are used in the design of a satellite communication link evaluation software package.

Chapter 3

Proposed Methodology

3.1 Introduction

In this chapter we define the scope of work planned. This is a combination of goals and achievements that would ultimately be used to determine the success of the project.

3.2 Simulation

The software package would start with the following inputs:

- Satellite TLE's
- Base station Latitude / Longitude co-ordinates.

These inputs would then be converted into two sets of Cartesian co-ordinates for the duration of simulation chosen. We can now calculate relative distances and angles between the satellite and base station at any point in time. Then, using the following further inputs:

- Communication frequencies used
- Satellite antenna gain
- Base station antenna type and antenna parameters

We can calculate the free space loss (FSL) and antenna gains for each pass. We also have the relative speed between the base station and the satellite at all times, which allows us to calculate the divergence in received frequency due to Doppler Shift. Other outputs would include visual representations of the orbit and further communications statistics.

3.3 Hardware

Two bench top QPSK transceivers would be designed and built. They would operate at two RF frequencies chosen to ICASA standards and an IF frequency chosen for ease of use and availability of components. The baseband ADC and DAC operations would be done by HvW [REF here] as part of another project. Certain design considerations would be taken to ensure correct integration between the two projects. All baseband and IF units would be PCB based. Each unit would also be allocated it's own PCB to simplify testing and debugging. All RF components would, if possible, be connectorised units. This includes amplifiers, filters, mixers, oscillators and antennas. Thus it is proposed that no detailed RF design would be done, only component specification and selection.

3.4 Doppler Shift Compensation

Circuitry would be added to one of the two transceivers that would attempt to measure the divergence in received frequency and try to compensate for it. Since the desired system layout chosen is a superhetrodyne transceiver, the IF frequency would be used. This relatively low frequency would be easier to work with than the particular RF frequencies and would contain the exact same frequency divergence.

3.5 Testing and Evaluation

Hardware

Each unit of the transceiver would be tested separately to ensure it complies with the design requirements. This would form part of the transceiver design results section. The quality of the communication channel created between the two transceivers would then be tested with the help of HvW [REF maybe]. This data rate and relative SNR ratios could then be compared with the theoretical values as calculated.

Doppler Shift Compensation

To test the operation of the Doppler shift compensation circuit with as little as possible external disturbances, the circuit would be connected to a QPSK signal generator. The modulation frequency of this generator would then be varied to replicate the effects of a satellite revolving around the earth.

At the output of the Doppler shift detection circuit, the difference in received signal frequency is measured by oscilloscope and also input to the compensation hardware. By comparing this measured signal with the transmitted

signal and observing the output generated by the compensation hardware, we can ensure that the Doppler shift detection circuit would work as intended.

3.6 Brief Summary and Prognosis for Next Chapter

With the proposed methodology and the full scope of the project, the next logical step is to design the satellite simulator software package.

Chapter 4

Simulator Design

4.1 Introduction

A common requirement for any communication link system design is specifying the correct hardware for the required data rates and reliability. Specifying power amplifiers that can transmit over the required distance, or an antenna with a wide enough beam width to allow for reliable reception. These are just some of the examples of the problems one faces when designing a communication link. As part of the transceiver design this masters project set out to accomplish, a software simulation tool was to be built to simplify some the decisions that would be required if the bench top transceivers we're actually used in satellite communication.

4.2 Objectives

The overall goal of this simulation tool is to help in the selection and specification process one goes through when selecting the front end components and antenna for both the ground station and the satellite. To achieve this goal, the tool would need to be able to do the following:

- Simulate a satellite passing through the field of view of a ground station
- Use different antenna types, with different beam widths / shapes, to calculate the exact reception duration
- Calculate the received noise and received signal power during this time of reception
- Give a statistical overview of the link performance for two week period of use, with a given transceiver layout

4.3 Program Operation

The operation of the simulator can be broken down into five sections, namely:

- Calculate antenna EIRP and other simulation preparations
- Satellite orbit and base station ground path calculations
- Determine signal reception durations
- Link quality and session duration calculations
- Visualizations of results

These five sections can be broken down further as shown in figure 4.1.

1: Collection of Simulator Inputs

The program has a wide range of inputs that need to be gathered. These are :

- Display options - Dual screen. detailed views etc.
- Antenna type and parameters (size etc.)
- Communication frequencies used
- Transceiver component gain / loss values.
- Transceiver component noise figures
- Antenna noise temperatures
- Base station location co-ordinates
- Required satellite TLE values (Eccentricity, Revolutions per day, Inclination)

The simulation parameters are defined in two steps: Increments and increment duration. The average simulation time was chosen as two weeks, since the simulation scenario repeats itself after this duration. The default time delta between simulation points is set at one second. This can however be changed to larger steps, for lower resolution results, but faster execution.

2: Calculation of Antenna Gain and EIRP

Depending on the selection done in the previous step, the EIRP of one of the four antenna types explained in section 2.3.9 are calculated. Except for the Yagi-Uda antenna, for which it was found easier to use a lookup table.

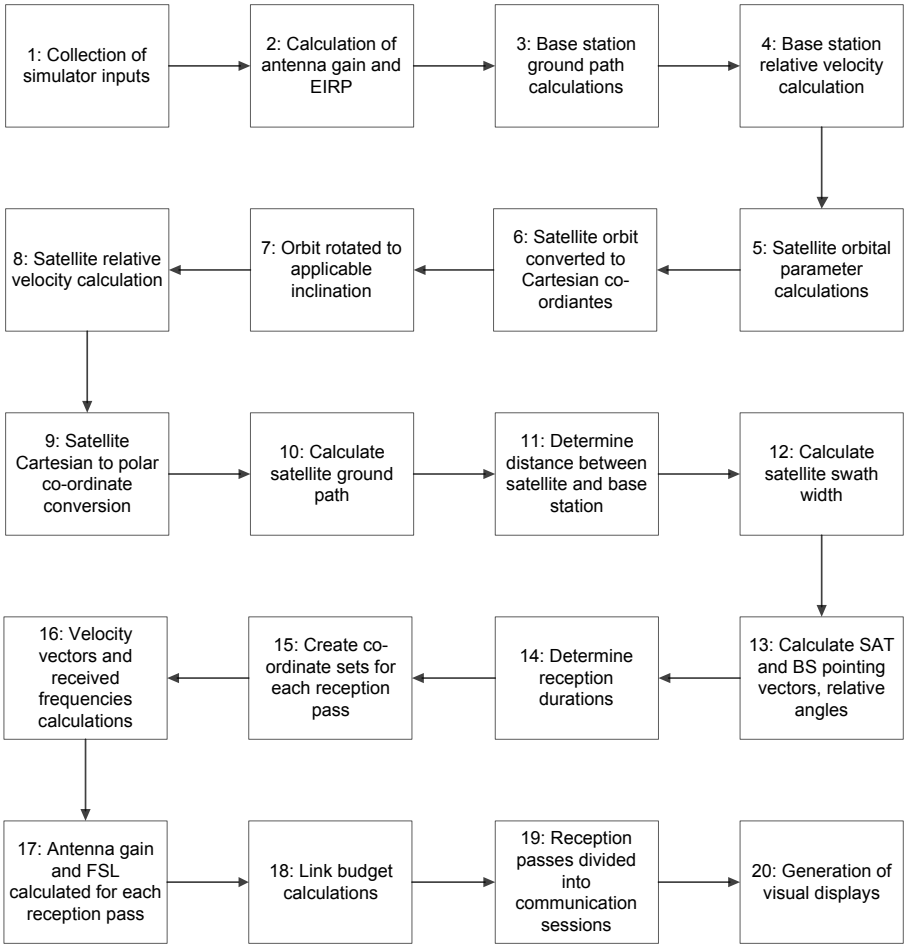

Figure 4.1: Simulation software operation flow diagram

3: Base Station Ground Path Calculations

Since the earth is not spherical, but an oblate spheroid, or oblate ellipsoid, the same basic parameters used to describe a satellite's orbit, can be used to describe the earth. The earth centered, earth fixed frame (ECEF) explain in section 2.2.4 was used to create a Cartesian set of co-ordinates using the starting lat/long values. The Longitude value was then updated by adding the angular velocity of the earth multiplied by the simulation incrimination described in step one above. By repeating this process for the entire simulation duration, we now have a set of Cartesian co-ordinates describing the base station location.

4: Base Station Relative Velocity Calculation

Even though the path traveled by the base station is not a straight line due to the curvature of the earth, for the small step size used this is a safe assumption. The relative velocity was calculated by subtracting the position of the BS at $t = x + 1$ from the position at time $t = x$

5: Satellite Orbital Parameter Calculations

Kepler's equations explained in section 2.2.1 allow us to calculate the velocity and coordinates of a satellite in terms the angle v. Since the required results need to be in the time domain, these equations need to be expanded and integrated to allow for a time domain simulation.

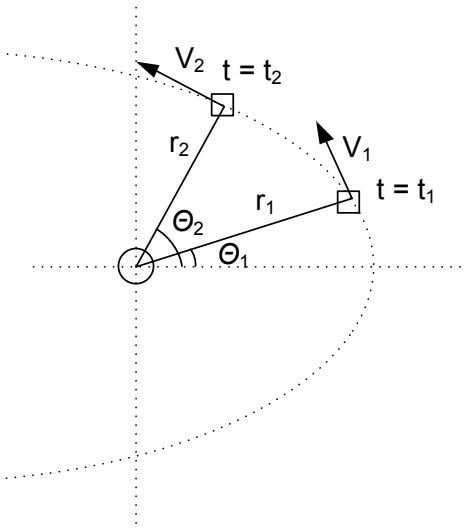

Figure 4.2: Two discrete steps in the orbit of a satellite

This is achieved by using an iterative process moving through the orbital path of a satellite in predefined time steps. A single iteration of this process, as shown in figure 4.2, works as follows :

1. r_1 using θ_1 and equation 2.2.2
2. v_1 using r_1 and equation 2.2.4
3. Calculate the distance traveled d by multiplying v_1 with the pre defined time step Δt

4. $\theta' = tan\left(\frac{d}{r_1}\right)$

5. $\theta_2 = \theta_1 + \theta'$

This generates r, v and θ values for the length of the simulation time required in steps of Δt.

6: Satellite Orbit Converted to Cartesian Co-ordinates

Every simulation incrementation now has a satellite orbit θ and r. These values are then converted to Cartesian x and y co-ordinates using basic trigonometry. The value of z is left as 0 since the orbit is only in two dimensions at this moment.

7: Orbit Rotated to Applicable Inclination

The rotation matrix described in section 2.2.5 is generated to perform a rotation around the y axis. The satellite inclination extracted from its TLE is used as the angle of rotation for this matrix. The set of Cartesian co-ordinates that describe the satellite orbit is multiplied with this matrix and a new rotated set of co-ordinates is created.

8: Satellite Relative Velocity Calculation

The same process as used in step 4, but this time using the rotated satellite co-ordinates.

9: Satellite Cartesian to Polar Co-ordinate Conversion

The new rotated Cartesian coordinates was now converted back to polar co-ordinates using equations 2.2.10.

10: Calculate Satellite Ground Path

The satellite latitude and longitude values calculated in step 9 were now used in equations 2.2.9. This generated a virtual ground path of the satellite in Cartesian coordinates.

11: Determine Distance Between Satellite and Base Station

The distance between the base station and satellite for the entire duration of the simulation was calculated. Basic trigonometry was used between the satellite and base station Cartesian data sets.

12: Calculate Satellite Swath Width

Using a mean earth radius of 6378000km we calculate the satellite field of view (Ω) angle, earth angle (ϕ) and swath width with the equations explained in section 2.2.2.

13: Calculate Satellite and Base Station Pointing vectors, Relative Angles

Usign the two sets of Cartesian values that represent the satellite and base station, we now calculate the following:

- Base station to satellite angles and distance
- Satellite to base station pointing vector
- Base station to satellite pointing vector

The base station to satellite angles and distances are calculated using basic trigonometry. The satellite to base station ($\bar{r}_{se}$) and base station to satellite ($\bar{r}_{es}$) pointing vectors are calculated as explained in section 2.3.1.

14: Determine Reception Durations

We now have all the data required to determine whether the satellite is in view of the base station and the duration of each pass. Communication is seen as possible when the following criteria has been met:

- The distance between the satellite ground path and the base station ground path are within the satellite swath width from one another.
- The angle between the satellite and the base station is smaller than the ground station antenna beam width.

15: Create Co-ordinate Sets for Each Reception Pass

Using the time values generated in step 14, we now create new data sets for the following:

- Base station Cartesian coordinates
- Satellite Cartesian coordinates
- Base station to satellite angles and distances (θ, ϕ and r)
- Satellite distance to ground
- Pass duration

16: Velocity Vectors and Received Frequency Calculations

We calculate the velocity vectors $\bar{V}_{SE}$ and $\bar{V}_{ES}$ by multiplying the relative velocities and pointing vectors as described by equation 2.3.5. With these velocity vectors we can now calculate the relative Doppler shift experienced by the transmitted frequencies as explained in section 2.3.1.

17: Antenna Gain and Free Space Loss Calculated for Each Reception Pass

Using the antenna EIRP values generated in step 2 and the base station to satellite angles calculated in step 15, the varying antenna gain for each pass is calculated. The distance between the satellite and base station (r), also generated in step 15, is used to calculate the free space loss (L_{FSL}) experienced during each pass. This is explained by equation 2.3.13.

18: Link Budget Calculations

Link budget calculations include the following:

- Received power calculations using an expanded Friis equation explained in section 2.3.11
- Base station and satellite antenna noise temperatures
- Receiver noise figures and received noise power for both transceivers
- SNR and Shannon limits for both transceivers

19: Reception Passes Divided Into Communications Sessions

Each satellite pass has a varying reception power for each pass. Each pass is divided into communication session bins of 10 seconds each. We can now count average communication session bins for the simulation duration.

20: Generation of Visual Displays

Figures are generated to display the calculated results and data. The following screens are displayed:

- A 3D representation of the satellite orbit and ground station for the simulation duration
- Dedicated statistics for each satellite pass which include : Base station antenna gain, FSL , Received frequencies and a 3D representation of the pass in question.

- Longest pass connection statistics : Height angle, Base station antenna gain, Distance between BS and SAT, FSL, SNR and Shannon theoretical data rates.
- Pass numbers and durations
- Session bins : Average received power per session vs the amount of sessions for uplink and downlink.
- Base station antenna EIRP
- Session display. A summary of results which include: Antenna EIRP, pass numbers and durations, Session bins

4.4 Discussion of Results

Due to the very specific design criteria of this software package, no single tool or methodology could be used to evaluate it's accuracy. The analysis was subsequently divided up into several parts.

Communication Analysis

To verify that the ground station antenna gain varied correctly with the passing of a satellite, a simulation was done with each of the supported antenna types and the same satellite orbital parameters. By then observing the relative antenna gain versus the influx angle experienced during a single pass, the correct operation could be confirmed. Another parameter which could be confirmed in this test is the free space loss (FSL) experienced, as well as its variation during the satellite flyover.

Shown below in figure 4.3 is the results of one of these verification tests. This specific test used a quadrifilar helix antenna for the base station. It's very wide influx angle is shown in figure A.22 in Appendix A.

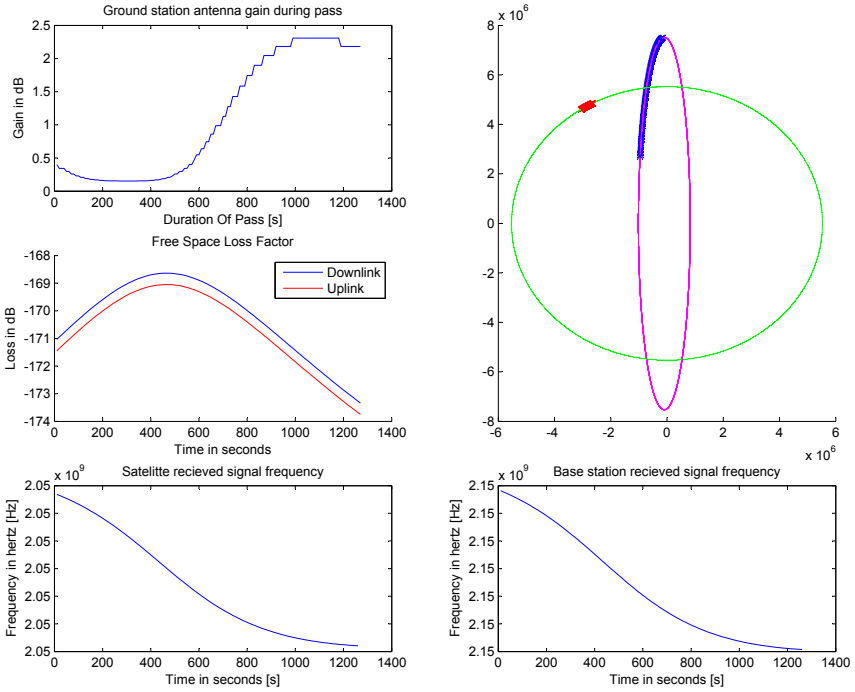

Figure 4.3: Simulator single pass statistics

A visualization of the satellite flyover can be seen in the top right image. The green path being that of the ground station, with red points indicating the base station position during the time of satellite visibility and the purple path being that of the satellite orbit, with the blue marks indicating it's location during visibility. The antenna gain variation during this pass is shown in the top left plot. For this specific antenna, we can see that the gain is low with the satellite directly above the ground station, this is the expected behavior for the quadrifilar antenna used. Similarly, we observe the variation in FSL for this pass in die middle left image.

Since the distance between the ground station and satellite vary as the satellite passes overhead, we expect the FSL to vary accordingly. This variation van be seen in the FSL plot, the middle left image in figure 4.3. By using the adapted Friis equation labeled as 2.3.11 in section two, we can calculate the absolute minimum FSL a satellite will experience. The example used here was the ISS, which has a orbital height of 400km. At this height and a perfect overhead pass, thus minimum distance between satellite and ground station, we get the following FSL values:

- FSL = 150dB @1.9GHz
- FSL = 171.7 @ 2.3GHz

The single pass shown above in figure 4.3 does not have a perfect overhead pass, instead this example showed an extreme case with the minimum distance between satellite and ground station being 3500km.

Orbital Mechanics

To ensure that the satellite orbits used for communications simulations are correct, orbital parameters generated by the software is compared with a well know, albeit quite old satellite software tool, Orbitron. [18]. The following satellites were used as a case studies for this check :

- ISS, Norad ID : 25544
- Cosmos 158 , Norad ID : 02802
- Globalstar M001,Norad ID : 25162
- Cosmos 1238, Norad ID : 12139

The simulated satellite orbital parameters, explain in section 2.2, were compared with the values generated by Orbitron. (Orbital period , eccentricity, velocity)

Doppler Shift

The maximum speed a LEO satellite achieves is at it's minimum height above the earth. While trying to keep atmospheric drag to a reasonable low, this speed is never higher than 7800m/s. For this worst case scenario, assume that this is in the exact opposite rotation of the earth and the base station is located on the equator. So it can now be shown that:

- $V_{EARTH} = \frac{\text{Circumference of the earth}}{\text{Duration of one rotation}} = \frac{2\times\pi\times6371}{23h56m} = 465.12\ m/s$
- $V_{SAT} = 7800\ m/s$

Thus our relative maximum speed between source and receiver, $V_{s,r}$, is equal to 8265 m/s. Using the the equations explained in section 2.3.1 we can calculate the maximum received frequency.

$$\Delta f = \frac{\Delta v}{c} f = \frac{8265 m/s}{299.792 Mm/s} \times 2.1\ GHz = 57.895\ kHz \approx 60\ kHz \quad (4.4.1)$$

These results were confirmed by creating a theoretical satellite with the given orbital parameters listed above, and simulating that satellite in the created satsim software. Thus this worst case scenario, in terms of Doppler shift,

can be simulated correctly. The average Doppler shift experienced was also compared for the list of satellites given in the previous section. All results were within the expected ranges these satellites would experience.

Additional Simulator Outputs

The software package also gave the user the ability to observe statistical data over an extended period. The ISS and a quadrifilar antenna was used for these demonstration plots.

Shown below in figure 4.4 is the session display generated. Top right is EIRP of the antenna used to generate the plot. Top left is the the amount of passes experienced over the simulation period, which is two weeks in this case. The bottom graph is a statistical display of communication sessions and their relative quality. It shows the amount of 10 second windows available for communication, at a verity of different received signal powers. This is under no means supposed to be valid communication circumstances, this scenario was selected to demonstrate the usefulness of the simulation tool.

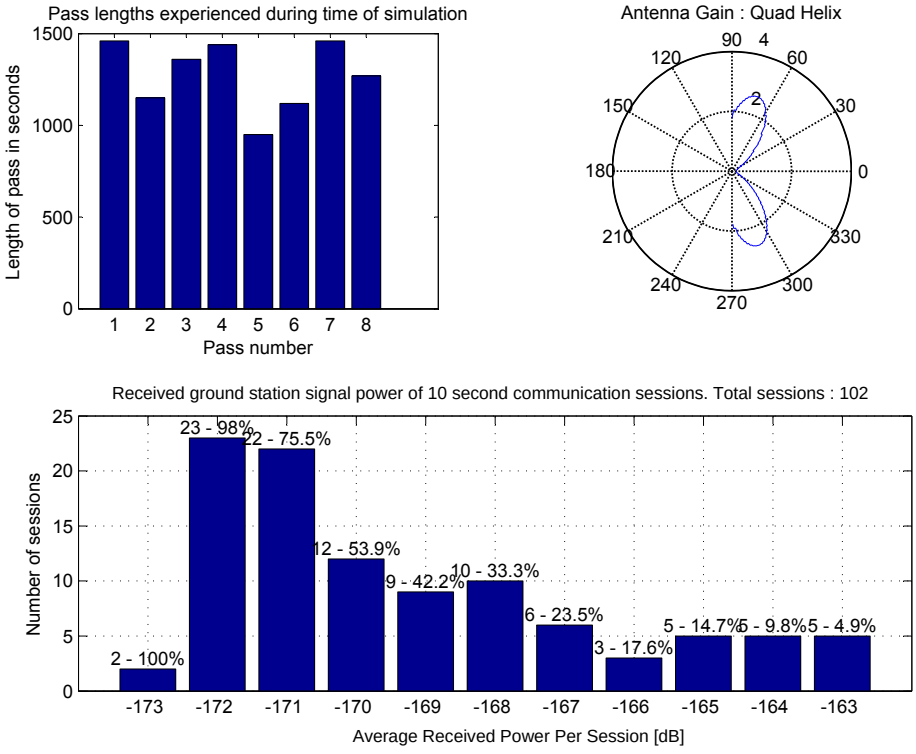

Figure 4.4: Session display and overview

4.5 Brief Summary and Prognosis for Next Chapter

Now that we have a general understanding of the circumstances under which a LEO satellite needs to communicate, we can look at the development of a QPSK transceiver which can operate under these same frequency and power constraints.

Chapter 5

Transceiver Design

5.1 Introduction

This chapter deals with the design of the S Band transceiver. The individual modules are designed and tested separately, with the results at the end of this chapter. A summary of all components used and operating parameters can be found in section 5.13.

5.2 Objectives

To achieve the goals as explained in the proposed methodology section, two development transceivers were designed and constructed with the following requirements :

- Create a channel of communication for two baseband signal inputs generated by existing hardware
- Modulate these signals and transmit them at an acceptable and relevant frequency.
- Replicate the variation in transmitted signal frequency that occurs due to Doppler shift in LEO to ground satellite communication.
- Receive and condition the transmitted signal.
- Compensate for the maximum Doppler shift generated.
- Demodulate, condition and output this compensated signal as two baseband signals.
- The components that make up the system would need to consist of detachable modules to allow for easy testing.

5.3 Proposed System Specifications

5.3.1 Transceiver Layout

One of the goals set for this project was to measure and compensate for the Doppler shift a LEO satellite experiences during a orbital pass. The standard method used in modern communication systems for Doppler shift compensation is to ensure that all channels and baseband conversion hardware can support the maximum and minimum frequencies experienced. Once the signal has been captured, the frequency shift is mixed up or down in software. In this project we attempted to measure and compensate for Doppler shift on a hardware level. Finding an easy method to do this could theoretically ease requirements on the downstream components of a transceiver, thus this requirement is purely for academic reasons and should not be seen as recommended practice.

Due to this constraint, a superhetrodyne transceiver layout was chosen. This layout allowed for more flexibility in terms of component selection and also gave a far more usable intermediate frequency to be used for any hardware designed to measure Doppler shift. Shown below in figure 5.1 is the proposed superhetrodyne transceiver layout, with the Doppler shift compensation circuit, which is explained in section 5.9.

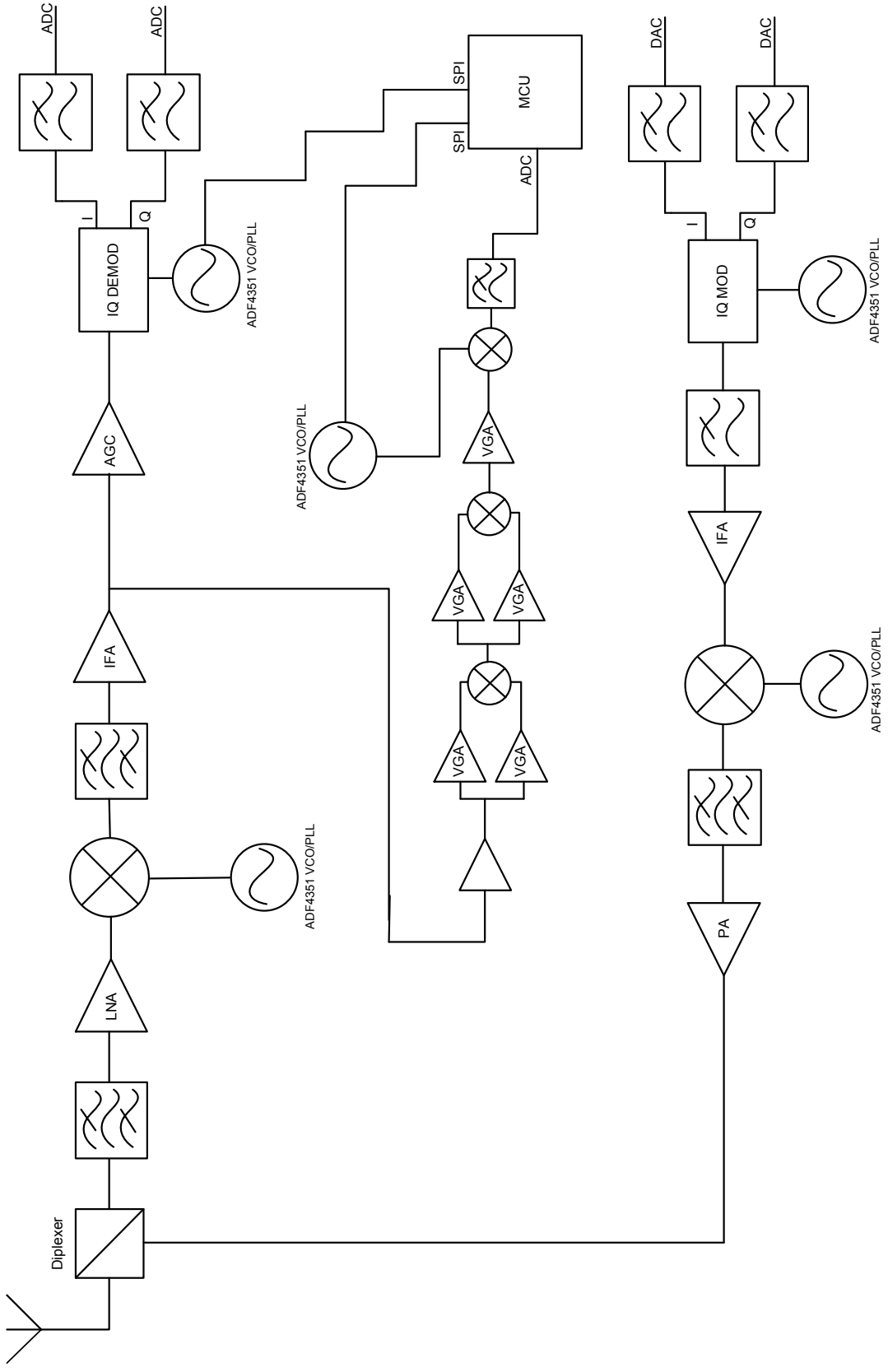

Figure 5.1: The proposed superhetrodyne transceiver layout

5.3.2 Operation Conditions

Transmission frequencies used

In section 2.3.7 an in depth description of the frequency allowances are explained. For this application the two carrier frequencies selected are : 2032.5MHz and 2207.5MHz.

System Bandwidth and Data Throughput

The specified data throughput given by Hendrik Van Wyk is 32kBps, thus a signal bandwidth of 64kHz. With the ICASA carrier frequency selection, a maximum channel bandwidth of 1.75MHz is allowed. Thus the transceiver will operate well within the ICASA bandwidth boundaries.

Channel Spacing

Since this is a channel application, channel spacing is not applicable.

Modulation Techniques / Levels

The modulation scheme specified by HVW is full duplex BPSK. In discussions with him, it was decided that since his baseband application could support M-ARY communication, it would be valuable to give the transceiver the same abilities.

Transmission Power

The purpose of this transceiver is to operate at the same frequencies as a transceiver would in LEO satellite communication, but under lab conditions. A appropriate power amplifier can be selected for bespoke satellite communication, but for this test setup nothing more than a safe 1W maximum output power is recommended.

Receiver Sensitivity

To achieve a reasonable data throughput with the given signal bandwidth of 64kHz, the final transceiver should achieve a Eb/No ratio of at least 15dB. This was seen as a sensible target to ensure that the hardware developed within this project is compatible with the system created by HvW.

5.4 Compatibility with Existing System

As described in the thesis document, Design and Construction of a Modem for Satellite Use by Hendrik van Wyk [19], the transceivers designed here would be supported by existing hardware designed by HvW.

Thus the inputs of this system would be generated by two ZTEX USB-XMEGA modules. The heart of these modules are a Atmel ATxmega128A1 processor, supported by a high speed USB link used for PC communication. The ATxmega128A1 supplies a adequate ADC and DAC interface used to generate and receive quadrature modulate signals [20]. The two PCs connected to these ZTEX devices run a software defined radio (SDR) software suite, designed in GNU radio by HvW.

The two baseband outputs that are generated by a ATxmega128A1 is modulated and mixed up to an intermediate frequency (henceforth referred to as IF). There the mixing harmonics are filtered out and mixed up to the chosen transmission frequency. Once at this high frequency, the signal is amplified and transmitted. The receiver operates in much of the same manner. The received signal is filtered and amplified by a LNA, and mixed down to the IF. Once the IF signal is filtered and amplified again, it is passed to a AGC amplifier and then a demodulator, as well as a Doppler shift compensation circuit. The demodulated signals are then captured by the second ATxmega128A1.

5.5 Baseband Design

The baseband signals would be generated and captured by ZTEX USB-XMEGA modules, supplied and operated by Hendrik van Wyk. The original design allowed for maximum baseband bandwidth of 200 kHz, since the expected highest signal component would be at 128 kHz. It was however discovered that the ZTEX modules can operate at far higher frequencies. To allow for further testing at higher data rates, a A Linear Technologies LTC1565 LPF IC was chosen as a suitable baseband filter IC, with a cut off frequency of 650 kHz [21]. This filter can also convert signals from differential to single ended, which was required since the ZTEX ADC had lower noise levels using a differential input.

5.6 Intermediate Frequency Design

The IF segment of the transceiver would take two baseband signals and modulate them to a quadrature modulated signal at the chosen IF frequency of 55 MHz. All connections between transceiver modules were achieved with SMA connectors and flexible RG-174/U flexible co-axial cable [22]. Since IF and baseband sections of the transceiver use relatively low frequencies, the impedance deviations that could be generated by PCB track widths, length and material were so small enough to ignore.

5.6.1 Modulator and IF LPF

The Quadrature modulation scheme chosen, in combination with the baseband layouts, allowed for various FM/PM schemes such as BPSK or higher M-ARY modulation schemes. This flexibility allowed the transceivers to be tested under a wide range of conditions and modulation schemes by HvW.

The modulator needed to operate at the chosen IF frequency of 55 MHz, be matched at 50Ω and required a external oscillator for testing and debugging purposes. The Mini-Circuits MIQC-88M+ was acquired, which is capable of DC-5 MHz input and 52-88 MHz output frequencies and allows for a maximum of 50 mW LO (Local Oscillator) Power [23].

The quadrature modulated signal output by the MIQC-88+ had to be filtered to remove the mixing harmonics generated by the the modulator. A Mini circuits PLP-70 was used to fulfill this role [24].

Once the IQ modulator/baseband filter design was finalized, it's theoretical power output could be calculated. This output power is described as:

$$P_{IQ} = P_I + P_Q - L_{MOD} \tag{5.6.1}$$

With P_I and P_Q as the input power supplied to the modulator and L_{MOD} as the conversion loss of 5.7 dB

The input powers P_I and P_Q can be discribed as:

$$P_I = P_Q = P_{avg} = \frac{A^2}{2R} \tag{5.6.2}$$

With the signal amplitude A , as 1 V_{p-p} and the input resistance R as 50Ω , P_I and P_Q can be calucalted as 2.5 mW or 3.98 dBm.

Using equation 5.6.1 and the power calculated above, we know that the IQ modulator has a ouput power of 2.26 dBm. This is further attenuated by the IF LPF by 0.48 dB, which brings the IQ modulator board's output power down to 1.78 dBm.

5.6.2 IF Amplifier

The modulator output power (calculated in section 5.6.1) of 1.78 dBm or 1.51 mW is far below the 50 mW maximum input power allowed by the RF mixers chosen in chapter 5.7.3. Since the carrier suppression of the mixer is constant in terms of input signal amplitude, increasing the input signal power would directly increase the signal to carrier ratio at the output.

To get closer to the maximum input power of 50 mW or 16.99 dBm, a Analog Devices ADL5601 gain block circuit was designed and implemented [25]. This SOT-89 packaged amplifier has a wide band fixed gain of 15 dB and is matched at 50Ω. Without taking any connector loss or impedance mismatch of the designed PCB into account, this amplifier would deliver 16.78 dBm, below the maximum of 16.99 dBm.

The final designed PCB was tested and had a gain of 15.5 dB at 55 MHz. With connector and co-axial cable losses taken into account the supplied power to the mixers were still below the 50 mW maximum. This concludes the transmission part of the IF segment of the transceiver.

5.6.3 IF BPF and Amplifier

After the signal is received and mixed down to IF, the superhetrodyte transceiver design requires a IF band pass filter (BPF) before the signal can be demodulated. This is necessary since it removes image frequencies created by the mixers and also removes out of band noise. Since this would be at the IF of 55 MHz, it was decided to pair the filter with a high gain amplifier on a PCB. The filter and amplifier would need 50 Ω input and output impedances to ensure maximum power transfer between transceiver modules.

The filter chosen was a Mini-Circuits PIF-50+ Constant Impedance Plug-In band pass filter, which has a pass band of 41-58 MHz and has a maximum input power rating of 500mW, which is well within it's field of operation [26]. This was matched with a Mini-Circuits AMP-76+ Plug-In low noise amplifier which has a typical gain of 26 dB, noise figure of 3.1 dB and operating frequency of 5-500 MHz [27].

5.6.4 AGC Amplifier Design

Following the IF BPF and amplifier, the final stage of the receiver required is a AGC (Automatic Gain Control) amplifier. Several Plug-In variations were considered to fulfill this role, but once it was realised that the Doppler shift compensation circuit would require several amplifiers, some with AGC, an easy to replicate lower cost PCB mounted amplifier was developed. The amplifier of choice was the AD8367, a VGA (Variable Gain Amplifier) with built in AGC [3]. This TSSOP Packaged amplifier has a linear in dB gain of -2.5 to 42.5 dB and a bandwidth of 500 MHz.

The operation of the amplifier is best explained by referring to it's functional diagram in Figure 5.2. The input is connected to a 200 Ω switchable attenuator network, which is in turn connected to a fixed 45 dB low noise amplifier. This mode of gain control allows for the lowest amount of noise present when the required amplifier gain is at it's peak. This attenuation is set by applying a voltage to the V_{gain} of the IC. This pin has two modes of operation as shown in figure 5.3 below .The mode of of operation is selected by connecting the MODE pin to either GND for LO or Vcc for HI.

As seen in the figure 5.3 , a lower voltage applied to V_{gain} gives a higher gain in LO mode, and vice versa in HI mode.

The second part of the AGC operation is the internal RMS detection circuit. This compares the output voltage with a calibrated set point of 354 mV

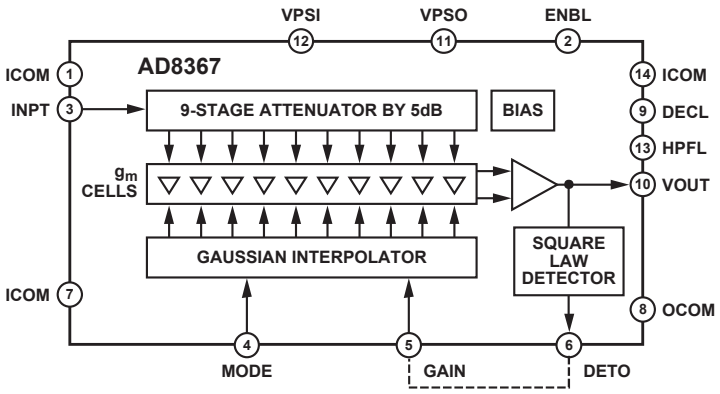

Figure 5.2: AD8367 functional diagram [3]

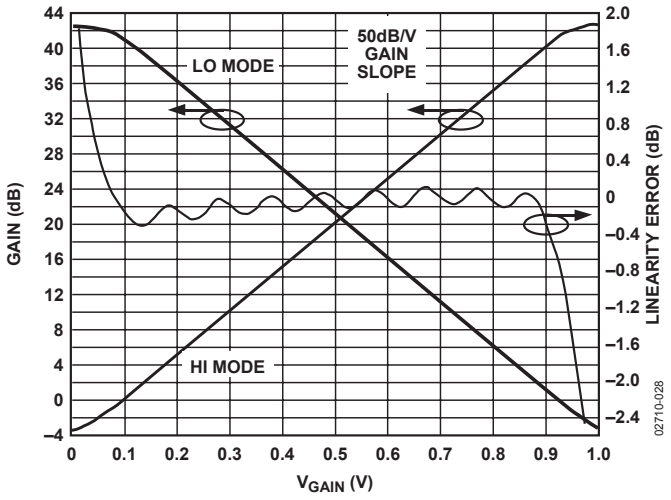

Figure 5.3: AD8367 gain vs V_{gain} input pin relationship [3]

rms. Any difference between these two generates a current that is integrated by an external capacitor connected to the DETO pin. This resulting voltage is used as the AGC bias and is fed back into the V_{gain} pin.

5.6.4.1 Prototype

To ensure that the AD8367 operates as described and that a working PCB layout could be achieved, the proposed Analog Devices prototype shown in figure 5.4 circuit was built and tested. Notice SW1 and SW2 in this figure.These switches allow for both AGC and VGA operation. A 10 kΩ variable resistor was used as a voltage divider between GND and Vcc to supply a voltage to the TP4 GAIN input. This allowed for easy VGA testing.

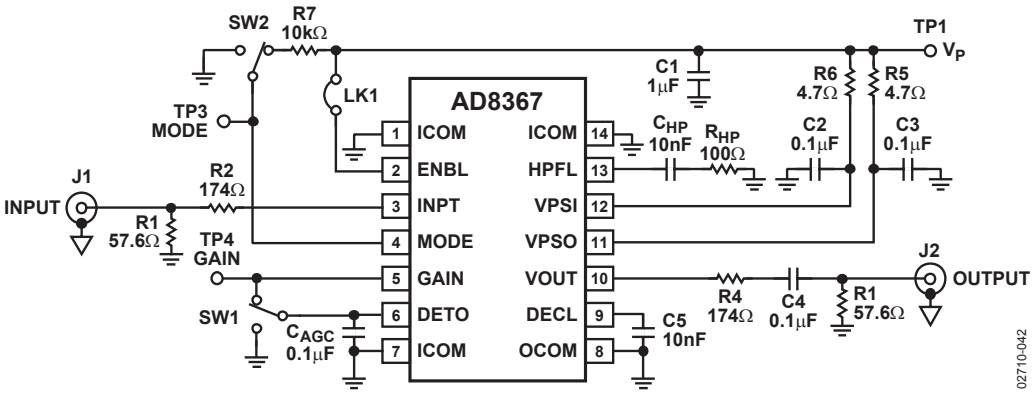

Figure 5.4: AD8367 evaluation circuit used as prototype [3]

5.6.4.2 Impedance matching and effect

The amplifier has an input impedance of 200Ω and an output impedance of 50Ω. Thus impedance matching was only required at the input of the amplifier. This layout can be observed below, in figure 5.5.

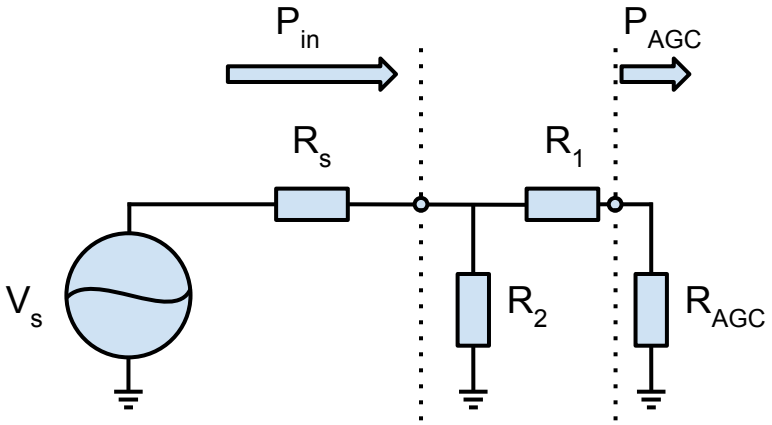

Figure 5.5: AD8367 evaluation circuit used as prototype

The reference design recommended a 62 Ω (R_2) resistor to ground at the input of the amplifier, in combination with a 178 Ω (R_1) series resistor. Effectively changing the amplifier impedance to 53.2 Ω.

The impedance matching done by adding resistors R_1 and R_2 minimizes the input reflection power that would've occurred if no matching were present. It does however lower the overall gain available. Lets define this loss due to impedance matching as L_{match}, which is calculated as:

$$L_{match} = \frac{P_{AGC}}{P_{IN}} \tag{5.6.3}$$

With the circuit and amplifier inputs P_{AGC} and P_{IN} shown in figure 5.5. By using the same annotation as shown in this figure, we can calculate the current flowing through R_s as:

$$I_s = \frac{V_s}{R_{total}} = \frac{V_s}{R_s + (R_2 || (R_1 + R_{AGC}))} \tag{5.6.4}$$

With this equation for I_s we can specify equations for P_{IN} and P_{AGC}. This is done below in equations ...

$$P_{IN} = RI_s^2 = I_s (R_2 || (R_1 + R_{AGC})) \tag{5.6.5}$$

and

$$P_{AGC} = R_{AGC} I_{AGC}^2 = R_{AGC} \left(I_s \frac{R_2}{R_1 + R_2 + R_{AGC}} \right)^2 \tag{5.6.6}$$

With these two equations we can calculate L_{match} using equation 5.6.3. With the chosen values of $R_1 = 62\ \Omega$ and $R_2 = 178\ \Omega$, we calculate L_{match} as 0.07455 or -11.28 dB loss. This loss factor reduces the maximum gain the AGC amplifier can supply from 42.5 dB to 31.22 dB.

5.6.5 Demodulator

The signal is has now been conditioned with the AGC circuit, and now needs to be demodulated. A Mini Circuits MIQC-60WD IQ demodulator was used [28]. This device is matched at 50 Ω and takes a quadrature modulated signal along with an oscillator, and delivers the two baseband signals originally generated by the modulator explained earlier. These two outputs are then fed into two of the same LTC1565 LPF used in the modulator segment of the transceiver. These filters generate a differential signal, which is then measured by the second ZTEX USB-XMEGA module.

5.7 High Frequency Design

To ease design and speed up completion of the overall transceiver system, connectorised modules were preferred for all high frequency components.

5.7.1 System Frequency Usage

The overall system would operate using four distinct frequencies with the transmitted frequencies as described in section 2.3.7.

- The baseband signal with a maximum bandwidth of 650 kHz
- Intermediate frequency of 55 MHz
- Uplink frequency of 2032.5 MHz
- Downlink frequency of 2207.5 MHz

5.7.2 Front End Design

The proposed front end of the transceiver would rely on two relatively wide band antennas and diplexers. Diplexers that work at the frequencies described in section 5.7.1 were available on the market. Unfortunately due to the highly specialized nature of diplexer design, the two frequencies initially selected for communication were not viable for this project.

Instead of using a diplexer and a single wide band antenna, a dual matched antenna layout , shown in figure 5.6. was chosen.To use this dual antenna system, and to move away from highly specialized filters, the uplink frequency was changed to **1900 MHz** and the downlink to **2300 MHz** respectively.

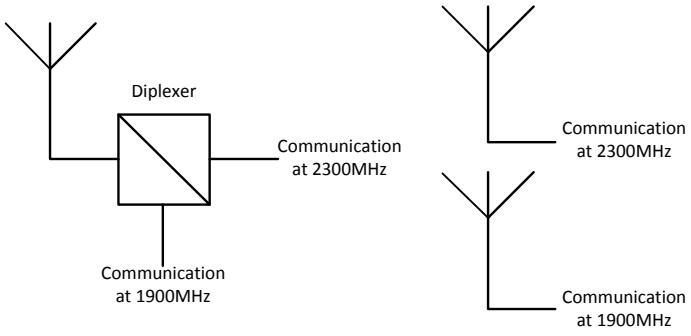

Figure 5.6: Original front end on the left, modified front end on the right

5.7.3 Wide Band Mixers

The superhetrodyne transceiver design required wide band mixers capable of up converting 55MHz to RF (either 1.9 GHz or 2.3 GHz) and the down conversion of the same frequencies. A Mini Circuits ZX05-43H wide band mixer filled this requirement [6]. It is a level 17 mixer, thus requiring an LO with an amplitude of 17 dBm. Operational IF frequencies range from DC to 1500 MHz , while the RF and LO frequencies can range from 1-4 GHz. The typical conversion loss is 7 dB for the frequencies used in this application.

5.7.4 Band Pass Filters

The original diplexed transceiver design required two sets of closely spaced narrow band pass filters to ensure correct operation. Since this was changed to a dual antenna design, the band pass filter selection became far simpler.

For ease of use and testing, connectorized Mini-Circuits filters were chosen. Listed below in table 5.1 are the chosen filters and their relative pass and stop bands.

Table 5.1: RF BPF Parameters [7] [8]

Name	Stop, Lower (MHz)	Pass (MHz)	Stop , Higher (MHz)
VBF-1945+	DC-1500	1850-2040	3600-5700
VBF-2275+	DC-1720	2170-2380	4200-6000

The listed pass bands of these filters have an attenuation of approximately 1.5-1.8dB and stop band attenuation of approximately 20 dB.

5.7.5 Low Noise Amplifier

The proposed system required two front end low noise amplifiers (LNA) which operate at the two respectable frequencies of 1.9 and 2.3 GHz. The connectorized Mini-Circuits ZX60-242LN+ fitted this perfectly [29]. It has a operating frequency of 1710-2400 Mhz and a low noise figure of 0.7dB for the chosen frequencies.

There is a slight variance in gain for the two chosen frequency bands, but 13.5 dB @ 1.9 GHz and 11.5 dB at 2.3 GHz is completely reasonable for this application.

5.7.6 Power Amplifier

The final stage of the transmitter design calls for a power amplifier. Since the effect of the transmitted power on the final received signal is well known and easy to calculate, a low power PA was chosen for the prototype system. An Analog Devices ADL5324 , with it's 400-4000MHz frequency range and 500mW maximum power delivery, fits this role perfectly[4].

The Analog Devices reference design circuit for the ADL5234 shown in figure 5.7 was designed, manufactured and populated. This reference design has variable positions for capacitors $C1^3$ and $C2^3$ which allows for variations of $\lambda 1^2$ and $\lambda 2^2$. These variable track lengths and interchangeable capacitors allows us to set the input and output impedance's for a specific operating frequency.

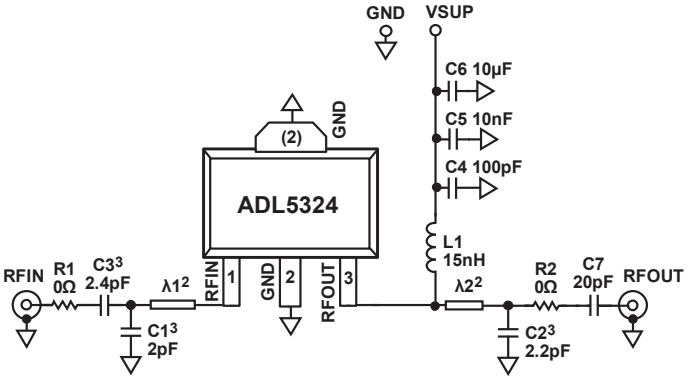

Figure 5.7: ADL5234 reference design schematic [4]

5.7.7 Antenna Design

The new layout design required two sets of antennas at different operating frequencies. All antennas that could be purchased at the time were either too cumbersome, too expensive or multi-band. (which would have lower gain and allow additional out of band noise)

To achieve the desired results in the short time span, it was decided to design and build antenna's for the application. The EMSS® antenna design software, Antenna Magus®, was used to create two circular patch antennas. The software takes several inputs and generates the antenna size parameters as shown in figure 5.8.

With FR4 as the material type and the two operating frequencies as 1.9 and 2.3 GHz, Antenna Magus gave the following antenna parameters, as shown in table 5.2:

Table 5.2: Patch Antenna Parameters

Antenna Frequency (GHz)	Substrate	D (mm)	Sf (mm)	H (mm)
1.9	FR4	43.6204	6.8075	1.5
2.3	FR4	39.3757	6.0747	1.5

Using the parameters from table 5.2 two patch antennas, with the layout shown in figure 5.8, were designed, etched and connectors soldered on.

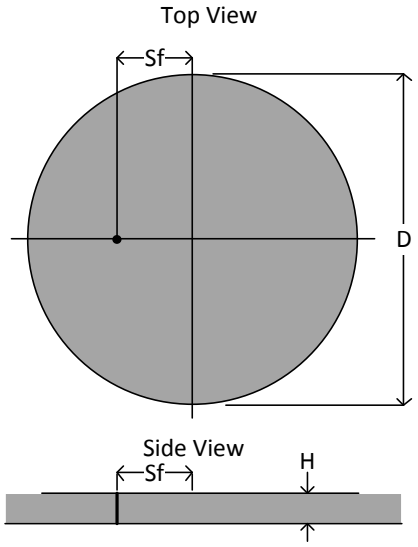

Figure 5.8: Circular patch antenna parameters

5.8 Wide Band Variable Oscillator Development

All the stages of signal conditioning described and designed so far rely on oscillators for mixing and modulation. Since the IF stage of the transceiver was developed first, it required a VCO that operates at appropriately 55 MHz. The original idea was to use Mini circuits Voltage Controlled oscillators, but extensive tests showed that this approach is too unstable and temperature dependent without a feedback circuit.

Since an oscillator circuit re-design was required and the superheterodyne transceiver design required further VCO's, it was decided to focus attention on a single very wide band VCO/PLL Combination.

5.8.1 Oscillator Requirements

The proposed transceiver design requires 4 oscillators,with a fifth used in the Doppler shift detector designed in section 5.9

- Static oscillator @ 55MHz for IQ Modulator
- Variable oscillator centred at 55 MHz variable with +/- 60kHz for IQ Demodulator
- Static oscillator 2245 MHz for 2.3 GHz up and down mixing

- Static oscillator 1845 MHz for 1.9 GHz up and down mixing
- Static oscillator @ 219.76 MHz for the Doppler shift detector

5.8.2 Analog Devices VCO/PLL - ADF4351

The ADF4351 is a "Wideband Synthesizer with integrated VCO" IC , powered by 3.3 V and programmed over SPI, this VCO/PLL combination offers an output frequency of 35 MHz to 4.4 GHz [5]. The IC also offers variable output power form -4 dBm to 5 dBm and very low phase noise.

These characteristics made it an ideal candidate to use for all the applications listed in section 5.8.1

5.8.3 ADF4351 Operation

As seen in figure 5.9, the basis of the ADF4351 is an integrated VCO with a frequency range of 2.2 tot 4.4 GHz and a divider circuit which can divide the output frequency by a maximum of 64, which allows for RF output frequencies as low as 35 MHz. This output signal is sent to $RF_{OUT}A$ and $RF_{OUT}B$, two differential adjustable gain power amplifiers.

The PLL segment of the device is supplied with a stable external reference frequency at REF_{IN}. The frequency of this clock signal can then be doubled, divided down by the R counter up to 1023 times and then further divided by a factor of 2 to supply a reference signal to the phase frequency detector (PFD). The RF N divider supplies the other input to the PFD. The N divider allows a division ratio in the feedback path, with it's input straight from the VCO / VCO output dividers. The PFD uses these two inputs to generate an output signal proportional to the relative phase and frequency differences. The PFD output, CP_{OUT} is then passed through an external filter circuit which is in turn used to set the VCO frequency, through V_{TUNE}. This is essentially the VCO/PLL operation. Two features which can also be seen in figure 5.9 are the lock detect LD and MUXOUT pins. The LD pin is pulled high once the PLL has achieved a stable state and the MUXOUT pin can be used to output internal signals of the ADF4351, perfect for debugging.

5.8.4 Device Programming

The programming of the device is done through a standard SPI port, with the three lines, CLK, DATA and LE, as shown in figure 5.9. The SPI port runs at 250 kHz , safely below the maximum speed of 60 MHz allowed by the ADF4351.

$$RF_{OUT} = f_{PFD} \times \left(INT + \frac{FRAC}{MOD} \right) \tag{5.8.1}$$

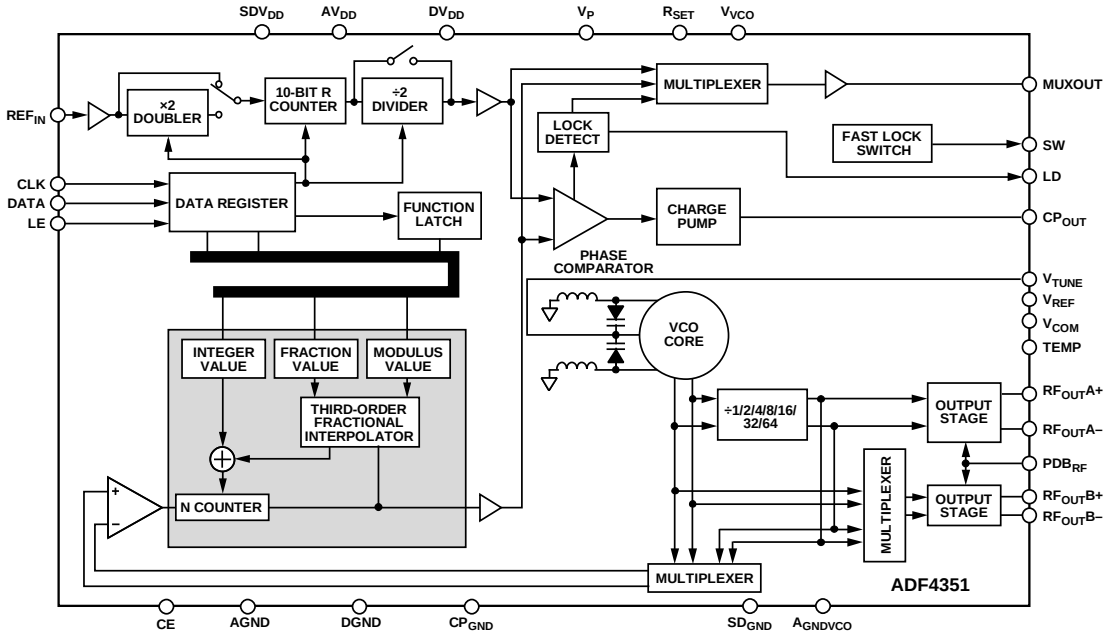

Figure 5.9: Functional diagram of the ADF4351 [5]

$$f_{PFD} = REF_{IN} \times \left[\frac{1+D}{R \times (1+T)}\right] \tag{5.8.2}$$

The VCO output frequency, RF_{OUT} can be calculated by substituting 5.8.2 into 5.8.1 and inserting the appropriate values for :

- INT is a 16 bit counter
- $FRAC$ is a 12 bit numerator for the fractional division
- MOD is a 12 bit modulus for the same fractional division
- D is the REF_{IN} frequency doubler bit
- R is a 10 bit divider ratio for the reference counter
- T is the REF_{IN} divided by 2 bit

This VCO frequency is then parsed through the buffer / divide -1/-2/-4/-8/-16/-32/-64 stage. This allows the final output frequency to be as low as 35 MHz, even though the VCO is operating at 2.2 GHz+. This signal then goes through the variable power amplifier stage to the differential outputs, $RF_{OUT}A$ and $RF_{OUT}B$.

These values and other specific operation parameters were calculated as shown in table 5.3 and are written to each VCO/PLL device on start up by writing the 6 different registers, as shown in figure B.1, to the device.

Table 5.3: ADF4351 Register values

$RF_{OUT}A$ Frequency (MHz)	INT	FRAC	FRAC (Final)	Divider
55	135	1575	1576	$^1/_{64}$
219.76	135	976	980	$^1/_{64}$
2245	86	1417	1422	$^1/_1$
1845	141	3780	3781	$^1/_2$

Since no two crystal oscillators are exactly the same, each VCO/PLL combination had to be calibrated to ensure the exact operation frequency. The value of MOD was set to it's highest which is 4095, to achieve the smallest possible step size. $FRAC$ was the adjusted until the correct output frequency were achieved, these values are listed in table 5.3 as FRAC (Final). The R counter was never required, thus R was set to 1.

The actual programming of each device was done with the SPI lines of the Atmel ATmega 256B. As seen in figure 5.17, a daisy chain layout was used for the MOSI and CLK lines, with each device having its own enable line. The 256B does have multiple SPI port support, but this solution was more elegant and simplified programming and PCB design.

5.8.5 Circuit Design

The reference design of for the ADF4351 was replicated with a couple of variations, chief amongst which was the addition of a ADL5602 gain block amplifier at one of the oscillator outputs. This configuration remained unchanged through all versions of the design. The first prototype circuit , left in figure 5.10 , had a Atmel ATMega 328P microprocessor to write the register values to the ADF4351 and a dedicated Texas Instruments TL1963A-33 3.3V LDO.

This prototype proved that the circuit design was correct and the device operated as expected. The final system would use at least four of these devices per transceiver, all programmed by a central MCU. This was the drive behind the second prototype shown in the middle of figure 5.10. It has header inputs for power and the SPI interface and an edge mount SMA connector for the RF output.

Once this design was proven correct, enough oscillators were produced to suite the needs of both transceivers. The unpopulated boards can be seen on the far right in figure 5.10 , with five completed oscillators to the left.

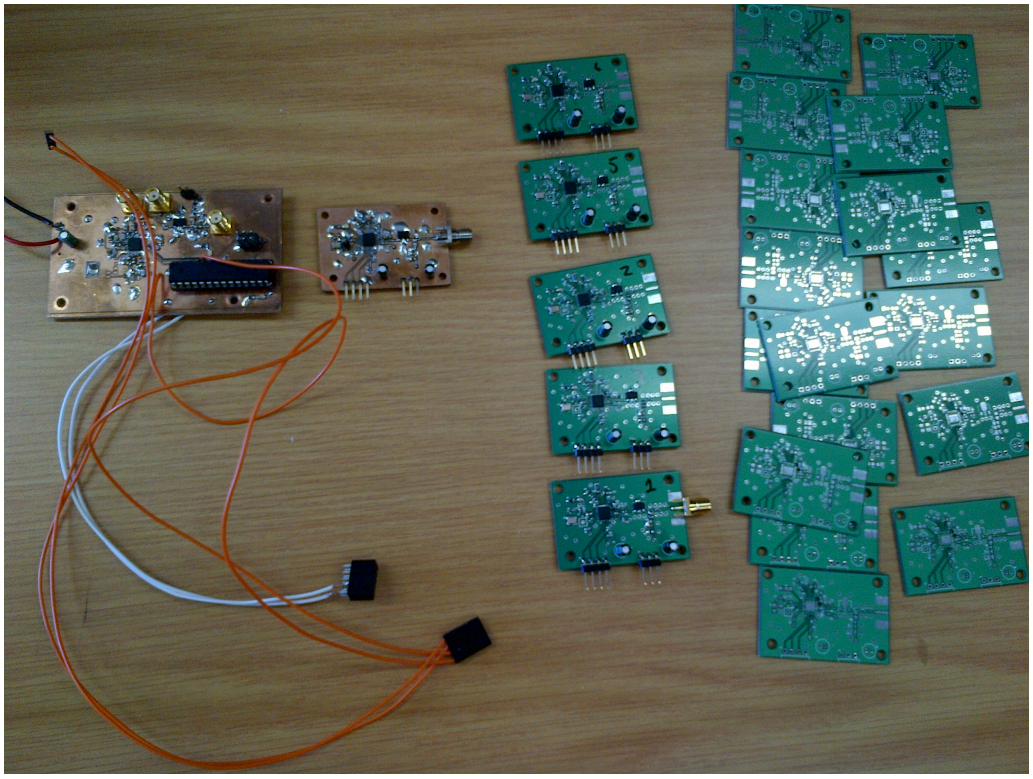

Figure 5.10: AD4351 prototypes and final manufactured oscillator/gain block combinations

5.9 Doppler Shift Compensation

As shown in section 2.3.1, any communication device operating in a non static environment will experience a relative Doppler shift in received frequency. Most modern receivers handle this by oversampling the received signal and compensating for it in software. Since the layout chosen was a superhetrodyne transceiver system and the oscillators were all variable, it was decided to handle this frequency variance in firmware and hardware.

The satellite simulation software created calculated the variance in received frequency due to Doppler shift, which can be seen in figure 5.11. As expected the frequency is higher than nominal as the satellite is approaching, exactly the carrier frequency for a brief moment and lower than nominal as it's moving away.

In simulations the highest shift in received frequency seemed to be around 40 kHz, but to ensure correct operation, the worst case scenario in terms of relative movement speeds needed to be taken into account.

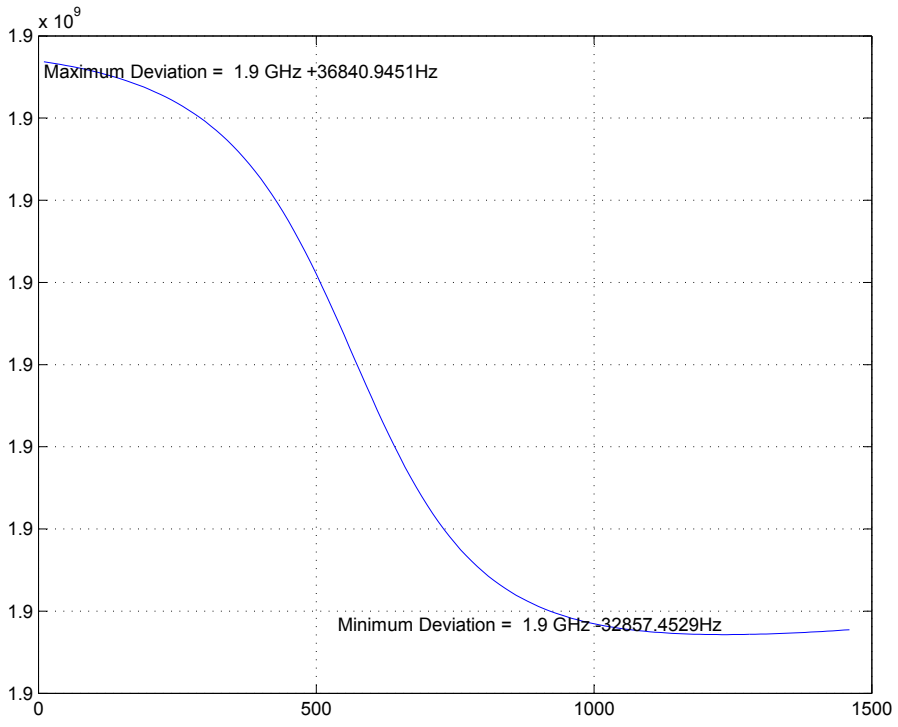

Figure 5.11: Received carrier frequency due to Doppler shift example from simulation software

This calculation was done in the verifcation of results section at the end of chapter 4. The highest doppler shift a satellite can experience is calculated in equation 4.4.1. This means that our final receiver segment needs to compensate for a frequency drift of $\pm 60kHz$.

5.9.1 System Operation

The input to the system would be the amplified IF signal at 55 MHz and the output would be adjusting the demodulator oscillator appropriately. A secondary output, a RS232 serial connection to a PC, was added for debugging and to ensure correct operation.

The system can be divided into two main parts:

- Shift extractor - A RF circuit that outputs the the Doppler shift frequency
- Frequency counter - Embedded device that detects shift and adjusts demodulator oscillator accordingly

Shift Extractor

Shown in figure 5.12 is the layout of the shift extractor and it's operation works as follows: The input to the shift calculator is taken directly after the IF amplifier / band pass filter stage. Since the output of this stage and the input of the demodulator stage are matched at 50 Ω, the calculator required a high input impedance, as to not interfere with communication system performance. This is achieved with first stage of the design, the buffer. Since the signal input to this circuit is a quadrature modulated signal and we're just interested in the deviation of the carrier frequency, the phase of the received signal had to be removed. Squaring a BPSK signal removes its phase component but also doubles it's frequency. in the same manner, taking a QAM signal to its fourth power removes the phase component and quadruples its frequency. The VGA amplifiers and and mixer that follow the buffer act as a signal squarer, the duplicate of this stage that follows takes the signal to its fourth power.

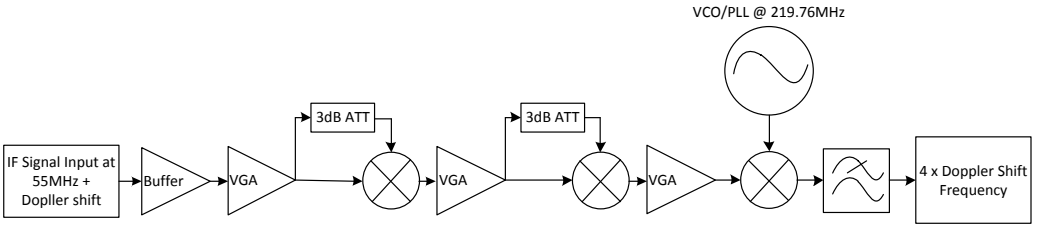

Figure 5.12: The proposed Doppler shift detection circuit

We now have the message signal at four times its original frequency but without it's variable phase component as seen in figure 5.13. It's important to realise that the effect of the Doppler shift is also multiplied by four.

We now remove the carrier component from the signal by mixing it down by 219.76 MHz. This produces a signal that can vary from 0Hz to 480 kHz , depending on the type of satellite orbit and relative speeds. Thus we now have a system that will output 240 kHz if the received signal is exactly 55 MHz and any variance from this carrier frequency is multiplied by four and added or subtracted from 240 kHz.

Frequency Counter

To complete the Doppler shift detection circuit we need to capture the shift detector output frequency and adapt the demodulator oscillator frequency. Using the ADC capabilities of an embedded MCU, the frequency offset could be counted and the demodulator oscillator set to its appropriate frequency, as seen in figure 5.14.

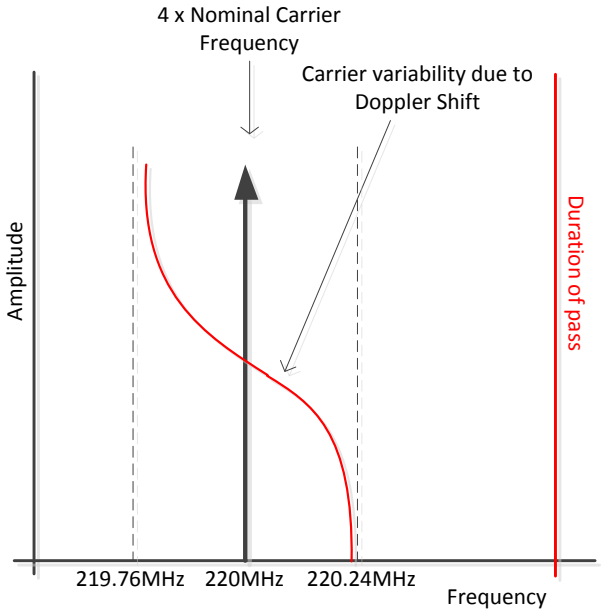

Figure 5.13: Frequency domain representation of the signal with maximum theoretical Doppler shift taken to it's fourth power

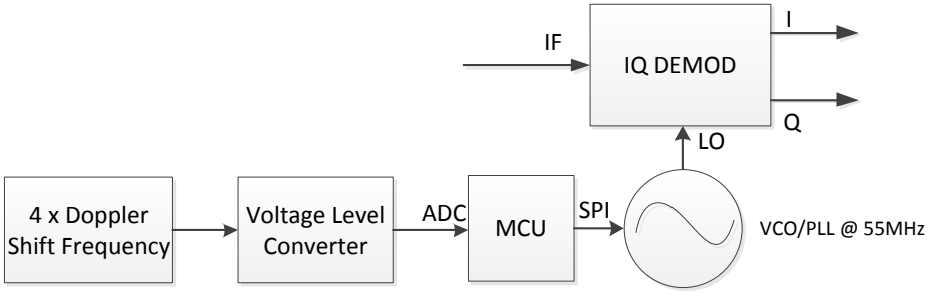

Figure 5.14: Frequency counter and compensator layout

5.9.2 MATLAB Simulations

To test the feasibility of the Doppler shift compensation system, a MatLab® Simulink® model was created. In essence, the proposed layout shown in figure 5.12 was built and simulated with the correct frequencies and filters.

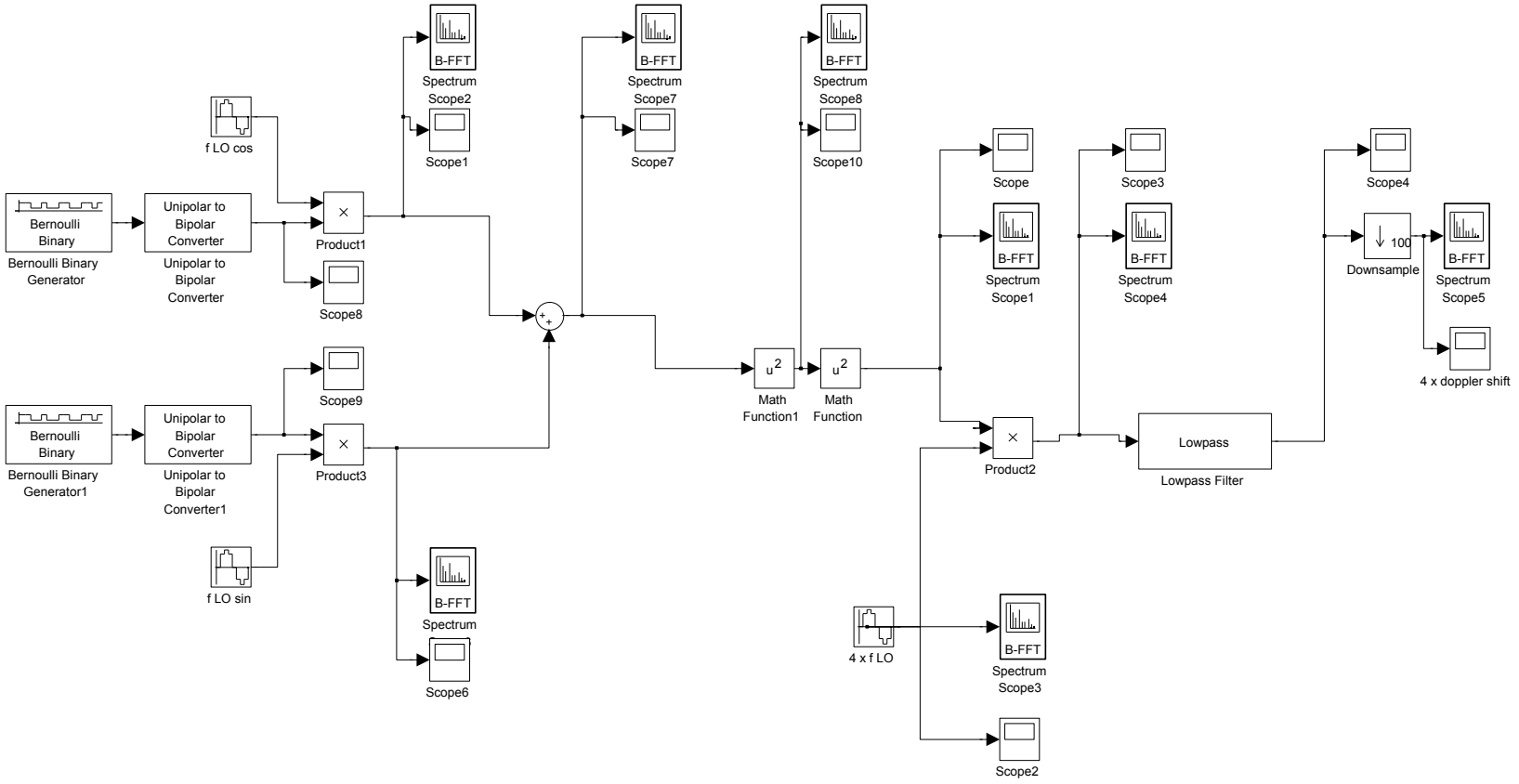

Figure 5.15: The Doppler shift detection circuit designed in Matlab

The simulation was run multiple times, changing the carrier frequency and observing the compensator output frequency. With a standard carrier input of 55 MHz the compensator has an output frequency of 240 kHz as seen in figure A.14. Figure A.15 shows the output when the oscillator is changed to 55.01 MHz which is 280 kHz, or four times the divergence from the standard oscillation frequency. This proves that the system would, at least in theory, work as expected.

5.9.3 Hardware Design and Implementation

Each segment of the compensator was designed and tested separately and built up in steps to achieve the overall layout. The final compensator circuit would consist of two PCB's, the MCU / frequency counter and the shift extractor. Thus all components used had to be surface mount or through hole. Schematics for these circuits can be found in appendix C, with the shift extractor as figure C.2 and the MCU as figure C.3.

Mini Circuits ADE-1L

This SMD mounted level 3 mixer has a frequency range of 0.5-500Mhz and a low conversion loss [30]. Tests done showed that the device performed as expected when used as a mixer, and that the device could be used as a signal squarer.

3dB Attenuator

The ADE-1L performs better when the LO power is higher than the IF power. Instead of using a VGA for both the IF and LO inputs, the IF input was put through an attenuator. More specifically a SSM 3 dB, 50 Ω PAT series chip attenuator.

Variable Gain Amplifiers

The AD8367 VGA/AGC amplifier circuit designed in section 5.6.4 was used to drive the mixers in the shift extractor. Minor changes were made to allow the amplifier to operate at a fixed gain or in it's AGC mode. This was achieved using jumpers LK1,LK2 and LK3 in figure 5.16. Connecting just LK3 enabled the previously designed AGC operation, while connection LK1 and LK2 allows VGA operation by supplying the GAIN pin with a voltage that can be set from 0-1V.

LPF

The post mixing filter required a cut-off frequency that allows the highest possible Doppler shift deviation through, thus a f_c of 480 kHz or higher. Since

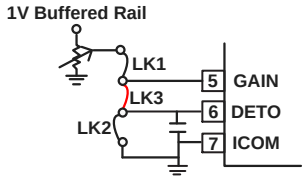

Figure 5.16: Modified AD8367 circuit that allows VGA operation

a reliable SMD filter with a f_c of 650 kHz was designed in section 5.5, the same filter and layout was used for the detector.

Buffered Voltage Rails

The compensator required two of it's own voltage rails. 1 V to power the potentiometers used to set the VGA amplifier gain and -2 V as a negative rail for the comparator described above. This was a achieved with two voltage follower circuits buffering the output of resistor network voltage dividers in a single AD8510 operational amplifier IC [31].

Input Buffer

The high input impedance of the shift extractor was achieved with a voltage follower op-amp circuit. A precision, low noise Analog Devices AD8610 operational amplifier fulfilled this requirement [32].

Voltage Level Converter

The output generated by the LPF swings around 0V and is sinusoidal. The MCU requires a square wave with specific maximum and minimum amplitudes. A voltage comparator was designed that would take the relatively small output of the LPF and convert it into a square wave signal with the correct amplitudes. The Atmel XMEGA 256B allows a minimum of -0.5 V and a maximum of 0.5 V above Vcc, which is 0.5 V above 3.3 V for this application. A voltage comparator circuit was built, with the negative input terminal connected to GND and the supply rails connected to 5 V and -2 V respectively. This generated a safe 3 V_{p-p} signal with a minimum voltage of -0.4 V. The actual performance of this comparator can be seen in the appendix, figure A.16. The level converter is grouped with the MCU in the documentation, since it's final operation is seen as part of the calculation circuity, but it was built on the shift extractor PCB. Thus the level converter is part of the shift extractor PCB and schematics.

System Requirements Upon MCU

The embedded micro controller had three basic roles in the compensation circuit. They are:

- Initialize ADL4351 VCO/PLL circuits
- The ability to count the rising edges of a square wave signal with a maximum frequency of 480 kHz.
- Use this counted frequency to calculate the new VCO frequency and the relative new register values for VCO/PLL.
- Write new register values to demodulator oscillator

These requirements were all fulfilled by the Atmel XMEGA 256B described in section 5.10

5.10 Microcontroller Selection and Design

The transceiver design required a embedded micro controller for the Doppler shift compensator and to program all other oscillators used.

5.10.1 Hardware Layout

The MCU chosen for this application was the Atmel Xmega 256B which was far too powerful in terms of processing power and peripherals, but was chosen due to availability and previous experience of the designer [33]. The 256B has four ports that can be dedicated to serial communication, two ports with ADC and DAC capabilities and other ports for programming, JTAG debugging etc.

The micro controller board required the following features / peripherals:

- A SPI port with several chip select (CS or LE for Load Enable) lines for the 4 static and one variable oscillator.
- An ADC input to be used for a frequency counter
- Output lines to power LED's as visual current state indicators
- UART to allow for RS232 serial communication. This was required for testing and debugging.

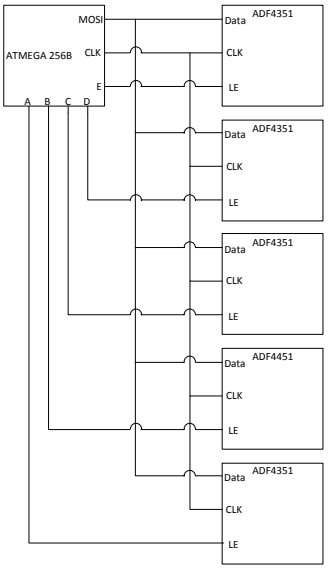

Figure 5.17: Programming bus layout between ADF4351 PPL units and Atmega 256B

SPI Interface

The correct register values of 5 different oscillators had to be written on start up and only the demodulator oscillator required constant adjustment via SPI. A single SPI port was utilised on the MCU and used in a programming bus configuration. As seen in figure 5.17, each oscillator was given it's own LE (Load Enable) pin and shared the common MOSI and CLK pins.

RS232 Serial Communication

Serial communication with a PC required a voltage level converter to change the 0-3.3 V UART to RS232 standard differential voltages. This was achieved with a Texas Instruments MAX2323 line driver, which uses a single 3.3-5.5 V supply voltage and a few additional components.

Other Peripherals

The LED circuit design was straight forward. With $V_{on} = 0.7\ V$ for a LED and a MCU operating voltage of 3.3 V, a 383Ω resistor in series with a MCU I/O gave a safe operating current of approximately 6.8 mA. The frequency counter abilities of the 256B allow the input to be connected to any of the device's I/O pins. An array of 8 LEDs were connected in this manner to port C of the MCU.

5.10.2 Software Operation

Frequency Counter

The 256B allows an input pin to be directly connected to the XMEGA Event system. The event channel output is routed to TCCB, a 16-bit timer/counter configured in a basic count-up mode. This operation can be seen in figure 5.18.A second 16-bit timer/counter, TCCA, is also configured as a simple count mode timer, but is connected to the CPU clock through a clock divider. This allows the frequency counter to adapt to a wide range of frequencies and resolutions.

As counter TCCA reaches its overflow (OVF), the 16-bit value in TCCB is latched into a 16-bit input capture register. The counter also allows for 32 bit operation in which TCCC starts counting once the TCCB overflow event occurs. Then instead of only using the value in TCCB when TCCA overflows, TCCB and TCCC are combined to give a 32 bit value.

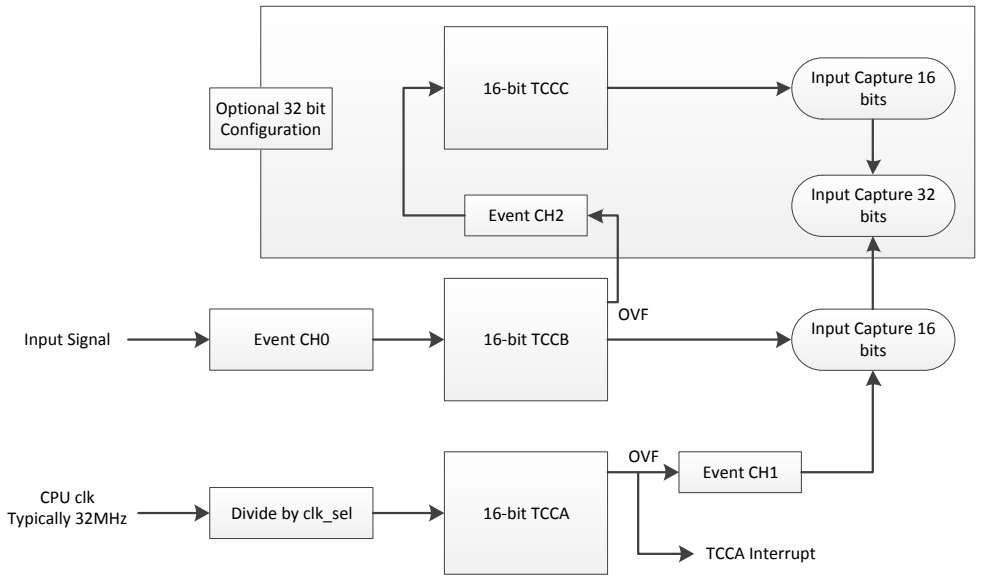

Figure 5.18: XMEGA frequenct counter layout

The maximum accuracy achievable with this frequency counter is in 32 bit operation. With this in mind, the clock divider can be selected for optimal counter accuracy and an acceptable frequency range. Shown in equation 5.10.1 is the calculation for the TCCA interrupt interval. This interval time deter-

mines both the maximum and minimum measurable frequencies.

$$\text{TCCA INT Interval} = \text{counter size} \times \frac{CPU\_clk}{clk\_sel} = 2^{16} \times \frac{32MHz}{clk\_sel} \quad (5.10.1)$$

The upper limit of the frequency counter is reached when both TCCB and TCCC overflows before the TCCA interrupt has triggered. The lower limit is reached when TCCB can't be reliably incremented at least once before the TCCA Interrupt. With these limitations in mind, clk_sel can now be chosen to allow an acceptable upper limit and a lowest possible lower limit that would give the best counter accuracy.

As stated above, the TCCC OVF occurs when both TCCB and TCCC have reached their maximum values before the TCCA interrupt has triggered. The maximum output of the frequency extractor is 480kHz.

$$f_H = \frac{\text{counter size}}{\text{TCCA INT interval}} = \frac{2^{16} + 2^{16}}{TCCAINTinterval} = \frac{\text{clk\_sel} \times 2(2^{16})}{2^{16} \times 32 \times 10^6} \quad (5.10.2)$$

With equation 5.10.2, the closest acceptable value of clk_sel can be calculated as 8, which gives a f_H of 500kHz.

Thus every 16.384ms the values of TCCB and TCCC are combined to give a 32 bit value. The minimum measurable frequency should have at least one rising edge during this count duration. This relates to a minimum countable frequency of $f_L = \frac{1}{16.384 \times 10^{-3}} = 61.035Hz$. Without averaging this is also the smallest frequency step size the system can measure.

SPI Initialization and Operation

The XMEGA 256B has four dedicated serial communications modules which support SPI. Each module consists of a baud rate generator, status and control logic with supporting registers listed below:

- SPI Control - This register sets the SPI operation parameters such as baud rate, master/slave etc.
- SPI Interrupt Control - These bits enable the SPI Interrupt and selects the interrupt level
- SPI Status - Contains interrupt and write collision flags used for data flow control
- SPI Data - Read/write register used in data transfers

With these registers, SPI communication was set up and used on port E of the MCU. To minimize possible errors in programming the PLL units due to external noise, the clock rate prescaler was set to $^1/_{64}$ which equates to a clock speed of 500kHz.

UART Initialization and Operation

As with the SPI communication explained above, a different serial communications module was set up to be used as a Universal Asynchronous Receiver/Transmitter (UART). Using the internal clock as a reference and setting the required registers, serial communication was achieved at 9600 bits per second.

5.10.2.1 Overall Software Operation

The MCU software operation can be broken down into three components, namely:

- PLL initialization
- Frequency counting and averaging
- Deviation calculation and PLL frequency adjustment

PLL Initialization

The four static and one variable oscillators are set up at their required frequencies and power levels.

Frequency Counting and Averaging

The frequency counter is started and is in fact in continuous operation. Once the TCCA overflow interrupt(explained in section 5.10.2) is triggered, the counted value is saved and the counters cleared. This counted value is then converted to Hertz and added to an averaging buffer. A average of 10 values is taken before moving on to the following stage.

Deviation Calculation and PLL Adjustment

The average frequency is then converted to its INT and FRAC values, and is then compared to the last values written to the PLL. If these values differ, the new register values are compiled and written to the device. If there is no variation, the frequency counting is resumed.

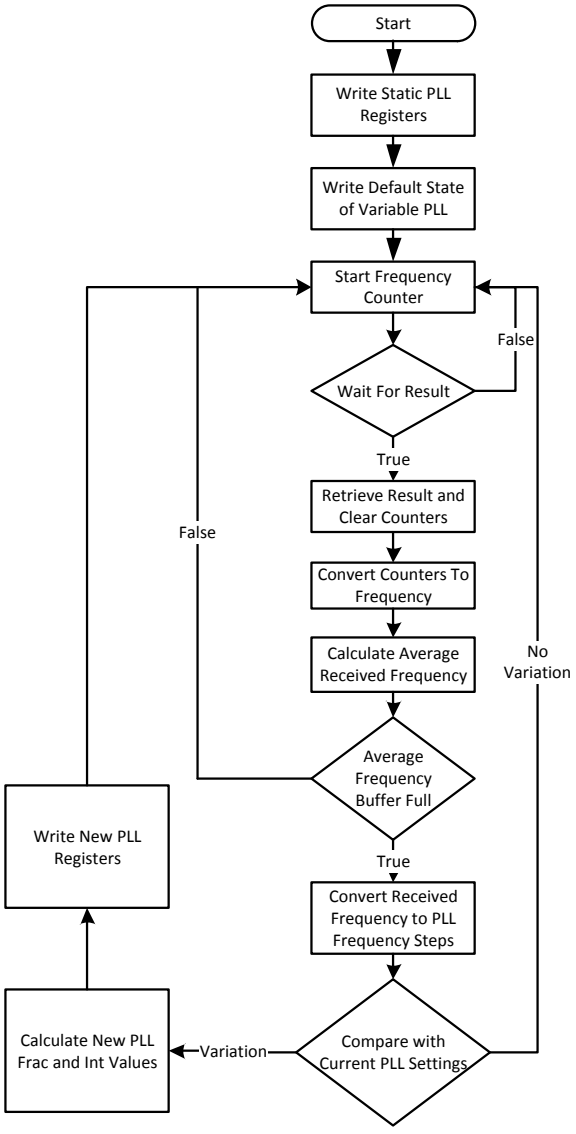

Figure 5.19: Embedded software operation flow diagram

5.11 Power Supply Overview

The transceiver component choices made required a array of different low noise and stable voltage sources. Since there were no efficiency limitation, a set of Low Drop-out linear voltage regulators (LDO's) were used to supply the required voltages. It was decided that each transceiver should operate off a single multi channel bench power supply. The two variable channels of this bench were set to +16V and -7V respectively. The bench also has a static 5V rail.

Below is a table of the required voltages and LDO's used.

Table 5.4: Voltage Regulators and Performance

Voltage (V)	LDO	LDO Max Current (A)	Package Type
3.3	TL1963A-33	1.5	SOT-223
5	REG104-5	1.5	SOT-223
-5	UCC384-5	0.5	SOIC
12	UA7812	1,5	TO-263
15	UA 7815	1.5	TO-263

The positive voltage regulator SMD package types listed above in table 5.4 all have a extra ground tab used for heat dissipation, thus using the copper on the PCB as a heat sink. To ensure safe continuous operation, a fan was added to cool the power tray PCB. The layout in terms of voltage rails can be seen in figure 5.20. The bench supply voltage rails are represented in red and the regulated and filtered output voltage rails are shown in green.

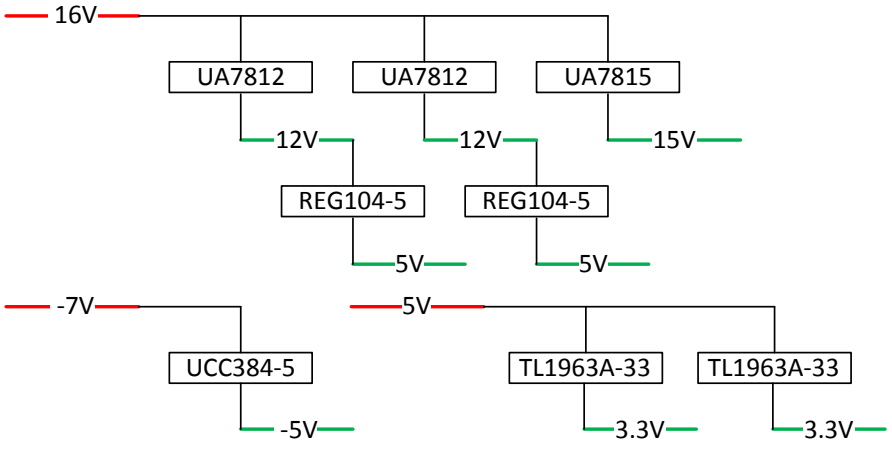

Figure 5.20: Power tray layout

5.12 Results

All components were tested separately to validate design parameters and to ensure correct operation.

5.12.1 AGC Performance

The prototype circuit underwent multiple tests. First among these was a wide band gain test on a vector analyzer, with the AGC switched off and the amplifier at it's maximum gain. The results of this can be seen below in figure 5.21. For this test a 40 dB attenuator was connected at the input of the amplifier, to test it's wide band gain factor (S_{21}). This shows a relative gain of 20 dB across the entire bandwidth. This gain is of course a lot lower that the stated 42.5 dB maximum gain. This was due to impedance mismatch since the AD8367 is made to operate in a 200 Ω environment, but is matched in this case to 50 Ω at both the input and output. Other factors that also contributed to this lower than expected gain factor are component tolerances. Care was taken during the vector analyzer tests to ensure that all cables and connector losses are accounted for, by following the correct calibration procedure.

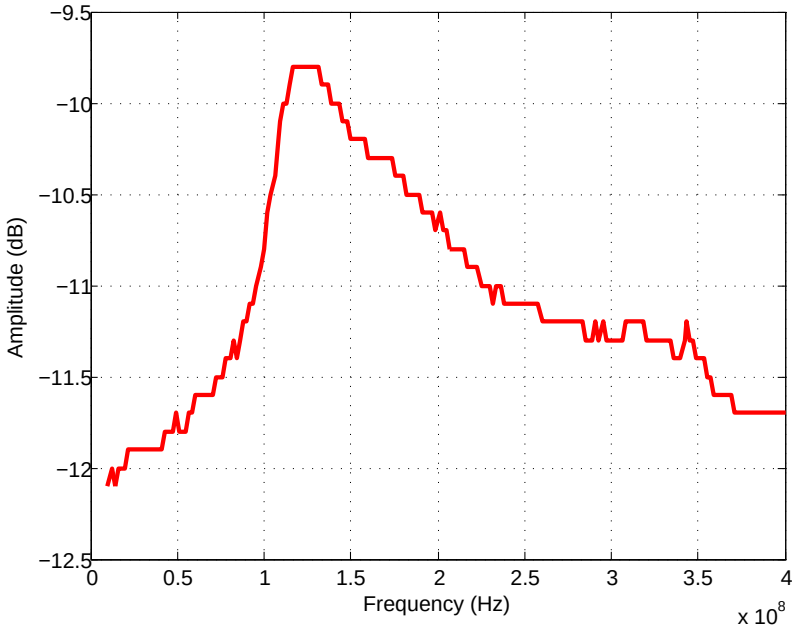

Figure 5.21: AD8367 Gain parameter measured with a Vector Analyzer

Secondly we needed to test the AGC operation of the amplifier. This was done by variang the input amplitude and observing the output. The device operated as expected up to the point where the equipment used to measure

the signal could not give furhter meaningfull results. The lowest sensible point captured can be seen in figure A.1 in Appendix A.

5.12.2 Antenna Performance

To test the efficiency and accuracy of the design, each individual antenna's input reflection coefficient (S_{11}) was tested on a vector analyser matched at 50 Ω.

Table 5.5: Patch Antenna Input Reflection Coefficients

Designed Frequency (GHz)	Antenna Number	Frequency of Lowest Reflection (GHz)
1.9	1	1.912
1.9	2	1.914
2.3	1	2.294
2.3	2	2.301

As seen in table 5.5, all four antennas performed well within $< 1\%$ of the designed operating frequency. The actual reflection coefficient graphs can be seen in the appendix, figures A.2 to A.5.

5.12.3 Doppler Shift Compensation Component Performance

The Doppler shift compensation circuit has several analog parts in the form of mixers, amplifiers and level converters. Shown below are the results of each individual component, tested separately.

IF Mixer

The ADE-1L mixer needed to fulfill several tasks in the shift compensation circuit. It was used as a signal squarer with inputs of 55 MHz and 110 MHz. Under these circumstances a 3 dB attenuator was connected to the IF input, since the LO input needed to be larger than the signal input for the mixer to operate correctly. It was also used as a down mixer to compare the quadrupled QPSK signal with the reference IC. The mixer was tested to unsure it operated under all these circumstances.

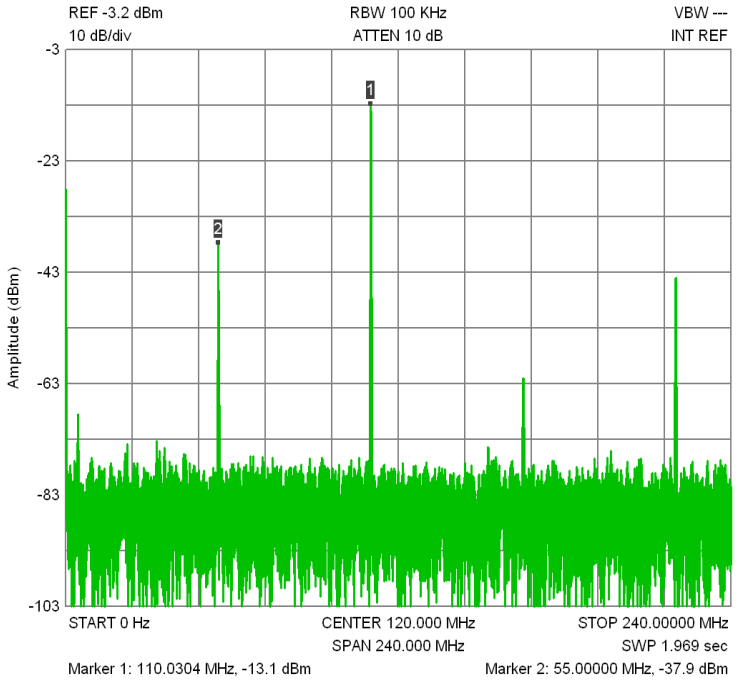

Figure 5.22: FFT of squaring a 55MHz Signal

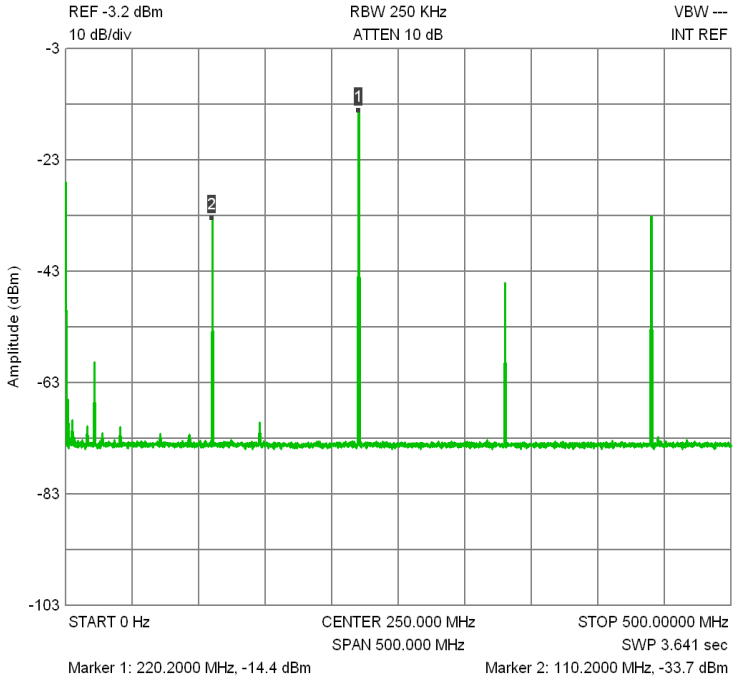

Figure 5.23: FFT of squaring a 110 MHz Signal

As expected, the mixer could act as a signal squarer. In both figure 5.22 and figure 5.23 the squared signal is shown using marker **1**. The other output to be aware of is marked as **2**. This is the input signal that leaks through to the output channel. The ADE-1L gives the typical oscillator suppression between 55 and 30 dB, with the suppression being worse at higher frequencies. Since the LO and IF inputs are the exact same signal when using the mixer as a signal squarer, this leaked signal is suspected to be slightly higher than expected when only taking the LO isolation into account. Other signals present are expected harmonic mixing harmonics. Also note that the FFT of the 110 MHz squared signal seems less noisy, but is not. This is due to averaging and larger frame sizes used on the FFT software when analyzing larger bandwidths.

Voltage Level Converter and Filter

This part of the circuit needed to filter frequencies outside of the expected range and convert the output into a wave with distinct rising edges, which would allow the MCU to count the generated signal frequency. When a sine wave with a frequency of 240 kHz and a low amplitude is input into the circuit, a near perfect square wave of the same frequency is output, but with an output swing between 0 and 3.5 V. This result is seen in figure 5.24. The same test is repeated with a input frequency outside the range of the filter. Shown in figure 5.25, we can see that the output of the filter still has a slight ripple, but the level converter does not trigger, giving the MCU a input that will be interpreted as a constant high.

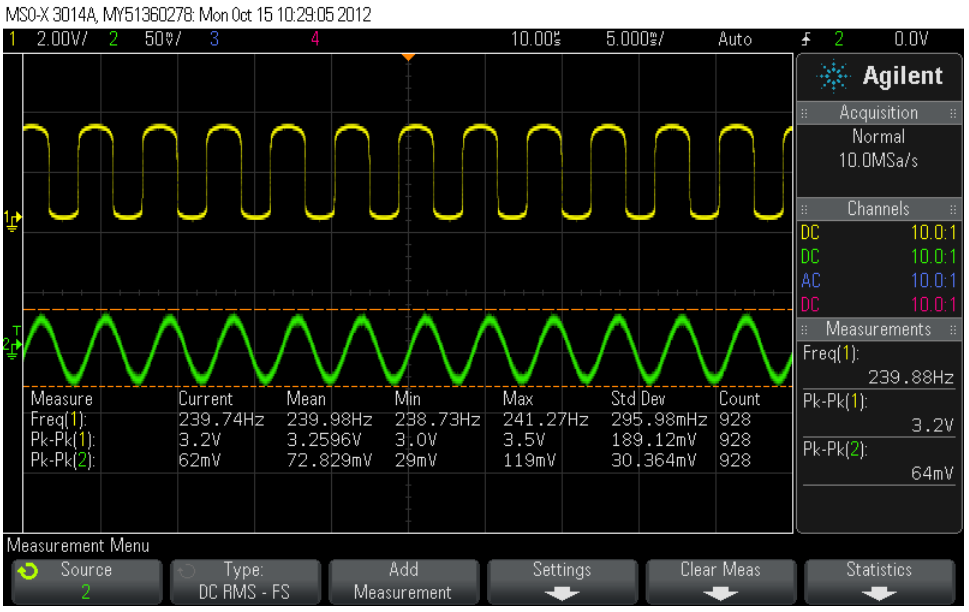

Figure 5.24: Voltage Level Converter and Filter output with an expectable input frequency

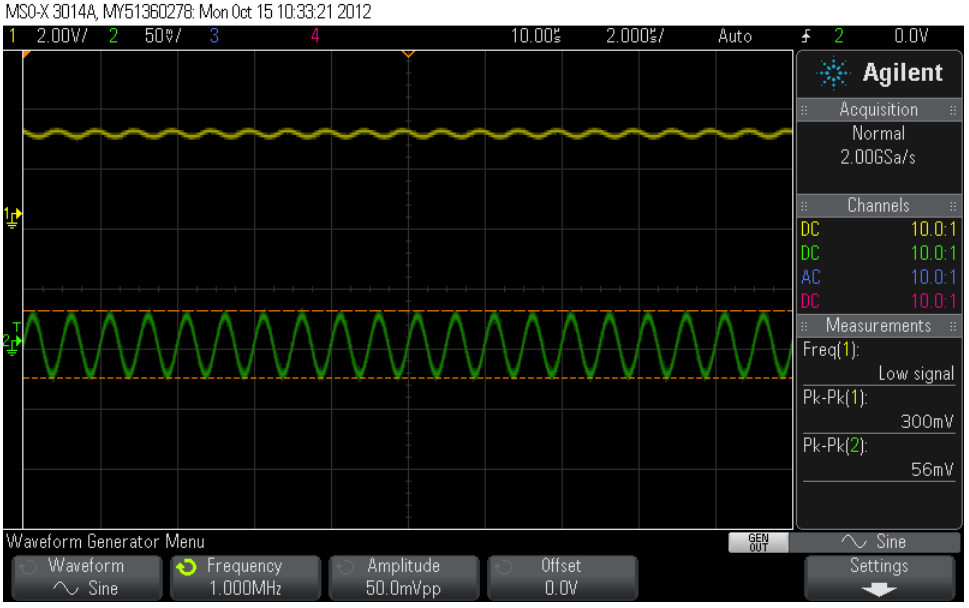

Figure 5.25: Voltage Level Converter and Filter output with an out of range input frequency

5.12.4 Baseband Filter Performance

Even though the LTC1565 Circuit was relatively simple, it was tested to ensure that its operation was correct and that the single ended to differential change worked as expected. The input frequency was incremented from 0 to 1.5 MHz and the attenuation was observed, with the results shown below in figure 5.26.

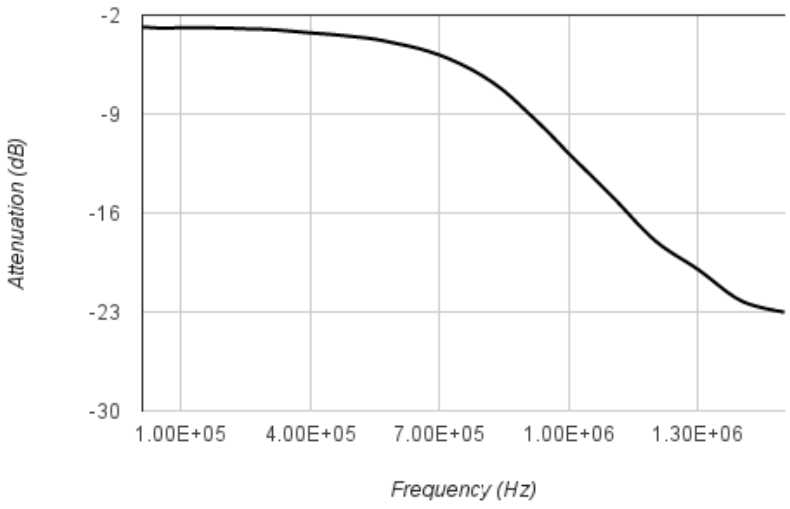

Figure 5.26: Attenuation vs frequency of the LTC1565 filter

5.12.5 IF Amplifier Performance

The IF amplifier performed exactly as expected, with a gain of between 14.5 and 15.5 dB at 55 MHz. Since the component implementation was simple and the operating frequency was relatively static and low (at 55 MHz), more detailed results were deemed unnecessary.

5.12.6 Power Amplifier Performance

The power amplifier PCB allowed for operating frequency selection. Thus one amplifier was tuned to operate at 1.9 GHz and the other at 2.3 GHz. Both amplifiers had a gain of approximately 11.5 dB at their selected frequencies. Below in figure 5.27 we see the gain vs frequency relationship of the power amplifier tuned at 1.9 GHz. Roughly the same performance curve was seen with the amplifier tuned at 2.3 GHz, where the device has a peak gain of 11.4 dB at the tuned frequency and gain decreases as the frequency deviates from

this peak.

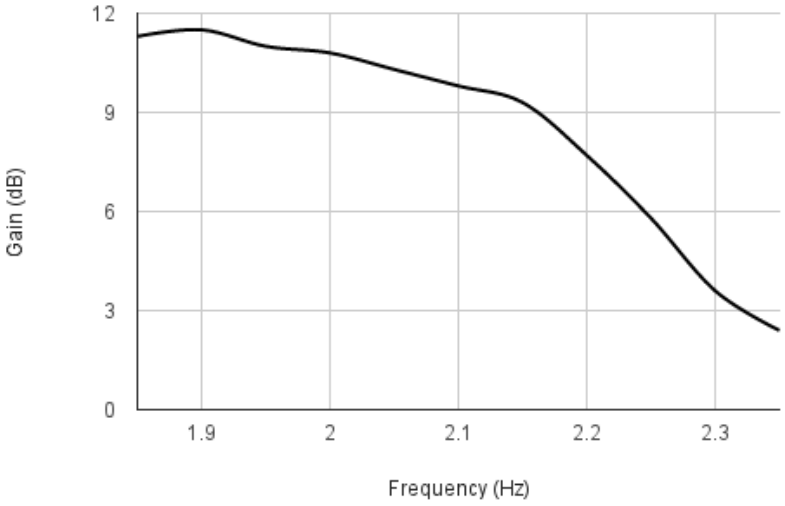

Figure 5.27: Gain vs frequency of the ADL5324 Power Amplifier

The gain of 11.5dB was not quite as high as the value indicated in the data sheet (Typical gain of 15 dB @1.935 GHz and 14.6 dB @ 2.140 GHz). The cause of this lower gain is suspected to be due to component tolerances, PCB trace lengths / component placement and connector losses.

5.12.7 VCO / PLL Performance

Several tests were done to ensure the operation of the device was suitable for the transceiver.

- Frequency range - Needs to operate at all required frequencies, from 55 MHz tot 2.245 GHz.
- Amplitude - Stable and variable amplitudes to power hi level HF mixers and low level modulators / demodulators
- Phase noise - Low phase noise at all frequencies to ensure stable operation

The results for these three parameters were obtained by doing two tests at each required frequency. Using a spectrum analyser the amplitude and phase noise was measured at each of the operating frequencies.

Table 5.6: ADF4351 Performance

Operating Frequency (MHz)	Amplitude (dB)	Phase Noise (dBc/Hz)				
		Average	100 Hz	1 kHz	10 kHz	100 kHz
55	18.5	-105	-90	-105	-115	-103
219.76	17.6	-102	-85	-105	-107	-104
1945	18.6	-90	-70	-84	-92	-92
2245	13.6	-85	-68	-85	-87	-90

Table 5.6 shows the designed oscillator design performance at all the required frequencies. The decay in maximum amplitude is due to impedance mismatch at the output of the device that occurs at higher frequencies. The captured data can be viewed in the appendix, figures A.6 to A.13.

The phase noise of the device is higher than the average noise given in the data sheet of the ADF4351, this is attributed to the addition of the ADL5602 at the output of the oscillator and further deviations in the components used.

5.12.8 Wide Band Mixer Performance

The ZX05-43H+ mixers selected for this project were thought to be matched at 50Ω for the selected frequencies of operation. This was not the case, with the component having far from ideal VSWR performance at the selected frequencies. As seen below in figure 5.28, the VSWR experienced at the selected operation frequencies are 3.8 for 1.9Ghz and 3 for 2.3GHz. This is assuming a LO power of 17dBm. The same unideal VSWR is experienced on the mixer IF port, this is shown in appendix A.19.

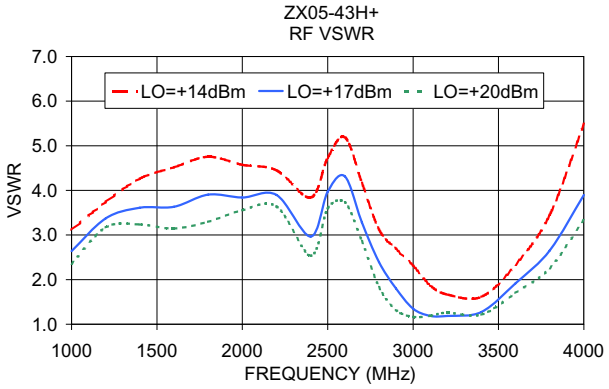

Figure 5.28: ZX05-43H+ RF VSWR [6]

An ideal RF VSWR of 1 would mean that there is a perfect power transfer between the component before the mixer and the mixer itself, similarly a IF VSWR of one would mean a perfect power transfer from the mixer to the next component in the signal chain. Since this is not the case with either port, the component is not being used under ideal circumstances, and the traditional calculation methods for noise temperature and component loss do not hold.

In chapter 2.3.6, we find the methods required to analyze a passive component being used under non ideal circumstances. The two aspects affected are the component loss and it's noise temperature. Firstly lets address the effect on loss.

Theoretical Wide band Mixer Loss

There are three loss components experienced by the mixer. $L_{IF-mismatch}$ and $L_{RF-mismatch}$, which are due to the impedance mismatches on the input and output of the mixer, and L_{conv}, which is the mixer conversion loss. L_{conv} can be read off the data sheet as 7dB for 1.9GHz and 6.5dB for 2.3GHz. The mismatch components can be calculated as follows:

- Read the port VSWR value
- Use the VSWR to calculate the reflection coefficient using equation 2.3.31
- With equation 2.3.32 and the reflection coefficient, calculate the loss experienced

With this process we get a $L_{RF-mismatch}$ of 1.806dB @ 1.9GHz and 1.249dB @ 2.3GHz. With a relatively small $L_{IF-mismatch}$ of 0.07dB @ 55MHz. This means the total component loss of 8.9dB at 1.9GHz and 7.8dB at 2.3GHz, with the total loss being a sum of the three parts. (conversion loss and reflection losses)

Theoretical Wide band Mixer Noise

The second aspect affected by the impedance mismatch is the mixer noise level. This updated equivalent noise temperature can be calculated with equation 2.3.29 in chapter 2.3.6. The two values required for this calculation are the reflection coefficient experienced and the component loss. Both of these values have been calculated above.

Thus the new component equivalent noise temperature for 1.9GHz can be calculated as:

$$T_{eq} = \frac{(7-1)(L+0.5833^2)}{7(1-0.5833^2)} T_0 = 2765K \tag{5.12.1}$$

Similarly we can show that the component noise temperature at 2.3GHz is 2208K.

Shown below is a summary of the previously assumed mixer performance under matched conditions versus the performance it will experience under the non ideal conditions it is implemented in this system:

Table 5.7: Mixer performance under matched and un-matched conditions

Frequency	Matched			Unmatched		
(GHz)	Loss (dB)	T_{eq} (K)	NF (dB)	Loss (dB)	T_{eq} (K)	NF (dB)
1.9	7	1163	7	8.9	2765	9.3
2.3	6.5	1005	6.5	7.8	2208	8.2

From table 5.8 we can see that the impedance mismatch experienced has a rather large effect on the component noise and loss. Since the mixer is at the input of the signal chain, this can have a rather large effect on the overall system performance.

Mixer Performance Measurements

To test the mixer under it's operating conditions, a QPSK signal was supplied with a 50dB attenuation to the LNA, which was in turn connected to the mixer. The output of the mixer was then measured with a spectrum analyzer with a input impedance of 50Ω. Shown in figure 5.29 is a FFT plot of the input QPSK signal supplied to the RF port of the mixer.

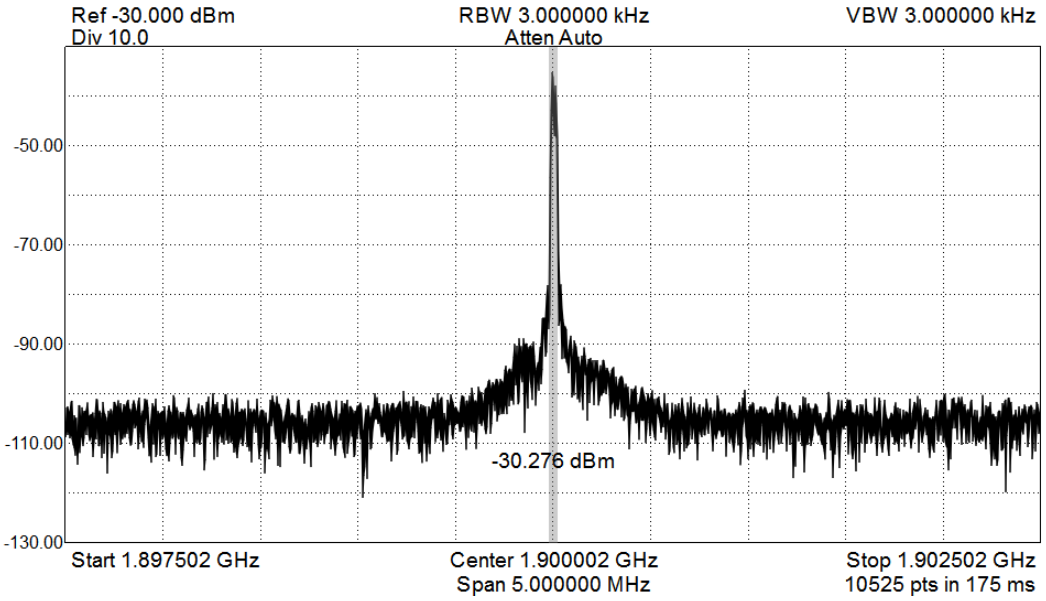

Figure 5.29: FFT of QPSK signal supplied to mixer

With a 17dBm LO supplied to the mixer, one can see the If output in figure 5.30 below. By comparing the peak power supplied to the mixer and the IF channel output it generates, we can measure the conversion loss, which is equal to approximately 10dB. This is slightly larger than the theoretical value calculated, but within expected bounds. This measurement was done for a 1.9GHz QPSK signal. The same process was repeated with a 2.3GHz signal, which generated a slightly lower conversion loss of 9dB, which is expected.

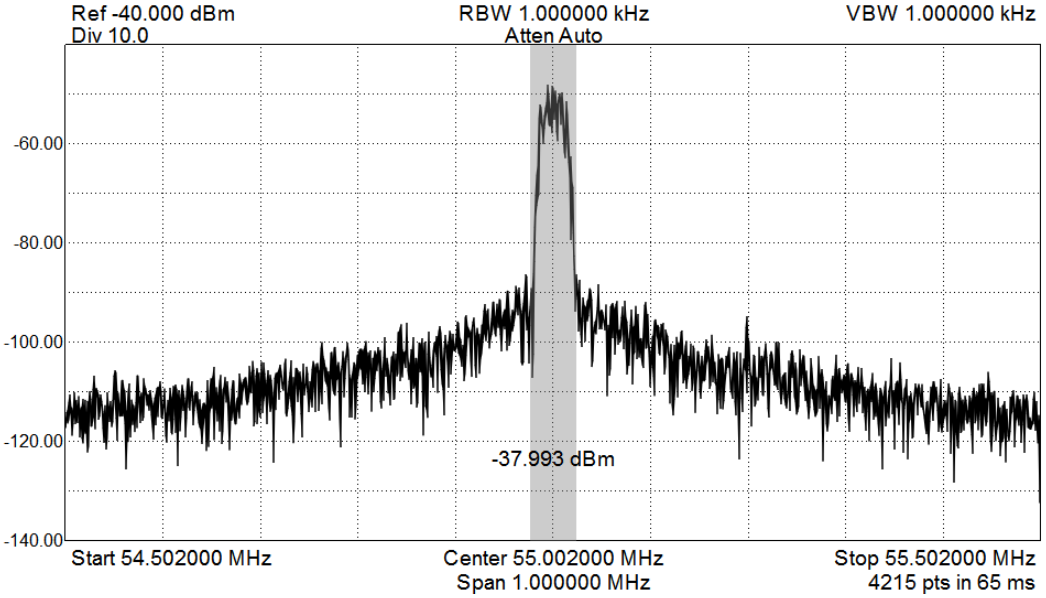

Figure 5.30: Narrow FFT of the IF output generated by the mixer, with a 1.9GHz QPSK signal as input

Lastly, shown below in figure 5.31, we can observe the full If port output with the same supplied 1.9GHz QPSK signal. As expected, there is a fair amount of LO leakage as well as RF leakage. These components are filtered out by the BPF following the mixer.

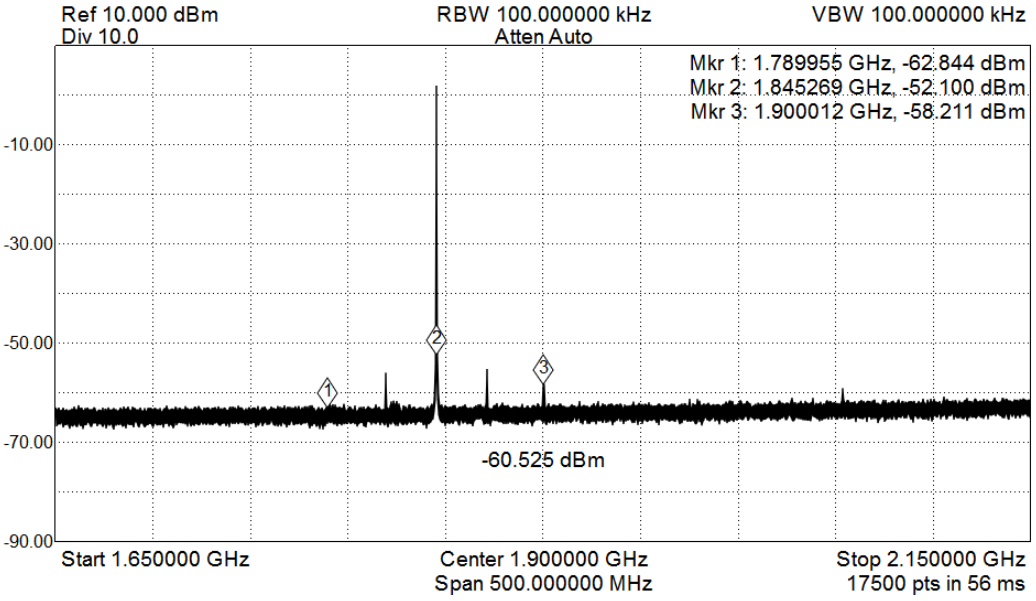

Figure 5.31: Wide FFT of the IF output generated by the mixer, with a 1.9GHz QPSK signal as input

5.12.9 Off The Shelf Components Performance

To ensure correct operation, all other off the shelf components were also tested separately.

Filters

The filters used in this system were impedance matched and tested. All results found were as expected. This includes the LPF and BPF modules.

LNA

By supplying the LNA with a QPSK signal at the chosen frequencies of operation, one could observe it's performance. Shown below in figure 5.32 is a 50dB attenuated QPSK signal supplied to the LNA, and in figure 5.33, the output generated.

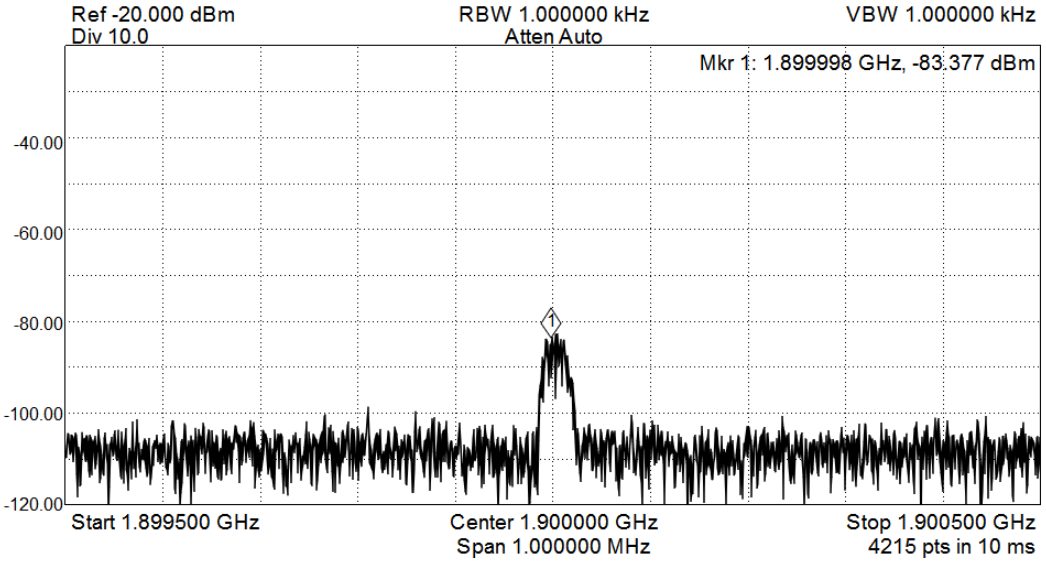

Figure 5.32: FFT of 50dB attenuated 1.9GHz QPSK signal supplied to the LNA

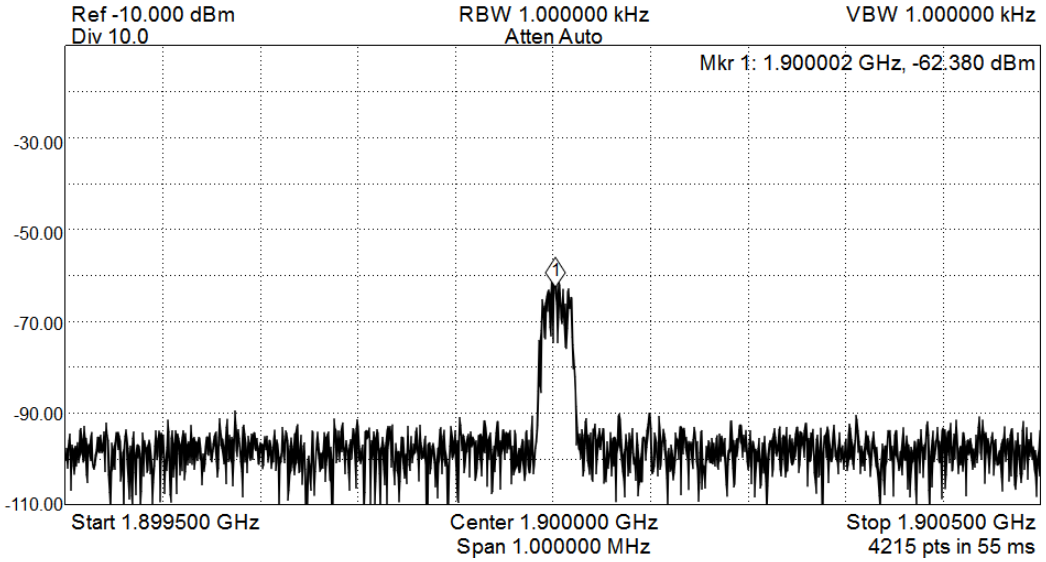

Figure 5.33: FFT output of LNA with a 50dB attenuated QPSK signal as input

With the 10 dB difference in reference amplitude, one can see that the LNA supplies a gain of 11dB at 1.9GHz. Similarly by observing the performance in figures A.21 and A.21 in appendix A, we can a gain of 11dB at 2.3GHz.

QPSK modulator / demodulator

These components were tested with support of the back end provided by HvW. A simple test setup was created to test the modulation and demodulation capabilities in the following manner:

- A PC running the SDR program was connected to the ZTEK module described in 5.4
- These modules are connected to the modulator, supplied with a 55MHz LO
- The modulated signal is sent through a LPF and supplied to the demodulator
- The demodulator is in turn also supplied with a 55MHz LO, the demodulated signal again supplied to a ZTEK module.
- This module is connected to a second PC, running the SDR program.

The SDR analysis done by HvW on this simplified BPSK system showed stable performance within the capabilities of the SDR frequency range. BPSK data rates of 128kBps were achieved with this method. Thus the baseband hardware could perform well within the required specification.

5.13 Component Specification Summary

Table 5.8: Component Selection Table

Designator	RF BPF CH1	RF BPF CH2	RF PA	RF LNA	MIXER
Part Number	VBF-1945+	VBF-2275+	ADL5424	ZX60-242LN+	ZX05-43H+
Frequency Range	1850 to 2040 MHz	2170 to 2380 MHz	400 to 4000 MHz	1710 to 2400 MHz	1 to 4 GHz
Loss / Gain (dB)	-2	-2	13.5 to 15.7	13	-6.5 to -9.3
Frequency Used	1.9GHz	2.3GHz	2.3GHz,1.9GHz	2.3GHz,1.9GHz	2.3GHz,1.9GHz
Specific Gain (dB)	-1.88	-1.51	14.1,15	12.5	-7.8, -8.9
NF (dB)	1.88	1.51	3.4, 3.6	0.64	8.2, 9.3
1dB comp (dBm)	-	-	29.1	16.5	-
IP3 (dBm)	-	-	43.1	32.5, 34.5	22
Designator	TX IFA	IF BPF	RX IFA	AGC	MOD
Part Number	ADL5601	PIF-50+	AMP-76	AD8367	MIQC-88M
Frequency Range	50 MHz to 4.0 GHz	41 to 58 MHz	5 to 500 MHz	DC to 500MHz	52 to 88 MHz
Loss / Gain (dB)	15	<-1	26	-2.5 to 42.5	-5.6 to -7.5
Frequency Used	2.3GHz,1.9GHz	55MHz	55 MHz	55MHz	55MHz
Specific Gain (dB)	15.6	-0.34	26.8	-13.78 to 31.22	-5.9
NF (dB)	3.9	0.34	3.1	52 to 6.2	5.9
1dB comp (dBm)	16.3	-	16.8	8.5	-
IP3 (dBm)	34	-	28	36.5	-
Designator	DEMOD	BBLPF			
Part Number	MIQC-60WD+	LTC1565-31			
Frequency Range	20-60 MHz	DC-650kHz			
Loss / Gain (dB)	-5.2 to -7	0 to -3			
Frequency Used	55MHz	128kHz			
Specific Gain (dB)	-5.3	0			
NF (dB)	5.3	-			
1dB comp (dBm)	-	-			
IP3 (dBm)	-	-			

5.14 Brief Summary and Prognosis for Next Chapter

With the transceiver design and individual component testing complete, we now need to look at the overall system performance. These are shown in chapter 6.

Chapter 6

Results

6.1 Introduction

All components of the transceiver were tested individually with their respective results shown at the end of chapter 5. In this chapter we focus on the performance of the completed system. The two aspects of operation we need to analyse are the transceiver performance and the operation of the Doppler shift compensation circuit.

6.2 Receiver Performance

To evaluate the performance and noise levels experienced in the system, the receiver RF to IF section of the reciever chain was tested separately. A Rhode and Swartz signal generator was used as a QPSK signal source, and measurements were taken with a vector analyzer.

6.2.1 Measurement Methodology

A input attenuation sweep was done from 30dB to 110dB, and the signal output at each connection point in the receiver chain was measured. Shown below is a sequence of plots taken to measure carrier to noise ratio (CNR) at an input attenuation of 50dB.

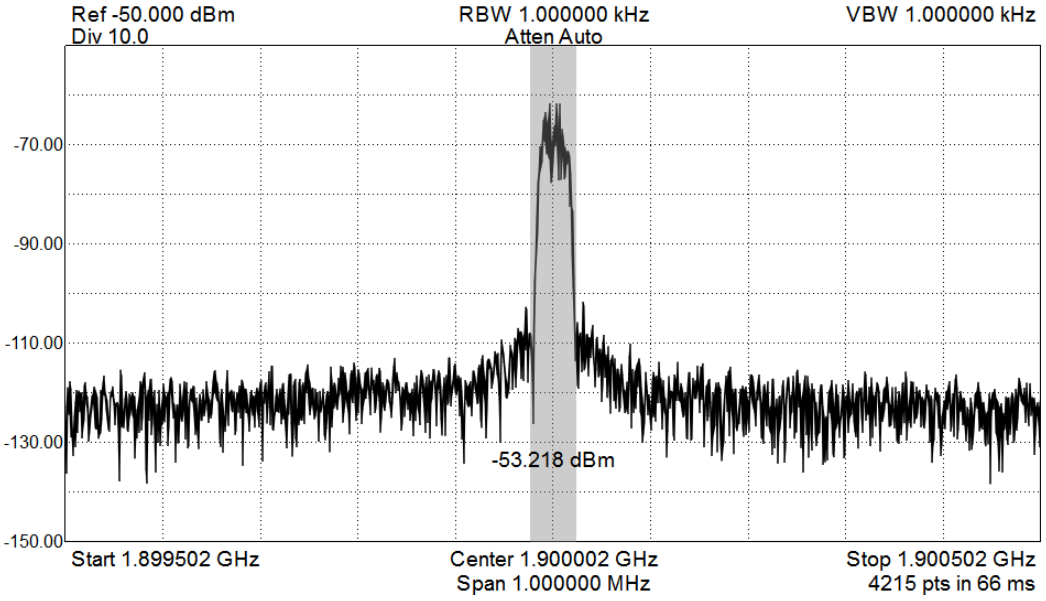

Figure 6.1: Receiver test input signal with an attenuation of 50dB

In figure 6.1 we see the system input applied to the receiver. By subtracting the noise floor from the channel power measured, we can calculate the approximate CNR ratio as :

$$CNR = \text{Carrier Channel Power} - \text{Noise level} = (-53) - (-110) = 57dB \tag{6.2.1}$$

The ZX05-43H mixer was then connected to the output of the LNA and supplied with a LO operating at 17dBm and 1845 MHz. The output spectrum is shown below in figure 6.3. Since this is a unfiltered passive mixer output, there are several other frequency components at this output port. For the purpose of SNR measurement, plot shows the part of the spectrum we are interested in. A full spectrum plot, which demonstrates the LO and RF leakage, as well as the image frequencies, can be seen in chapter 5.12.8, figure 5.31.

This signal, with image frequencies and other mixer induced components is the connected to the IF BPF and amplifier circuit. These two components are not separable, thus their measurement is a combination of the two components.

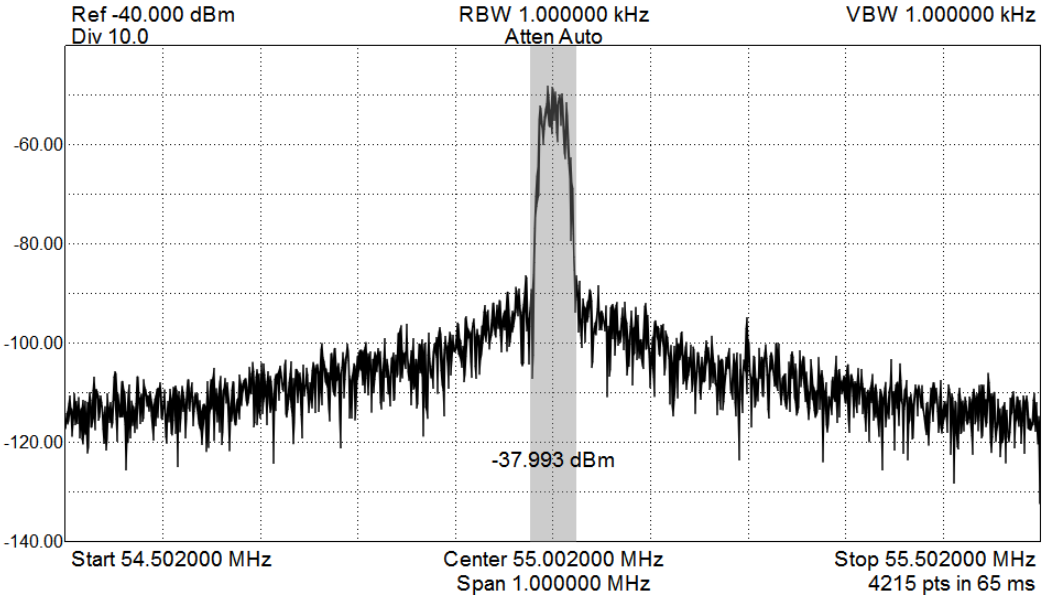

Figure 6.2: IF QPSK signal measured at mixer output, with a system input attenuation of 50dB

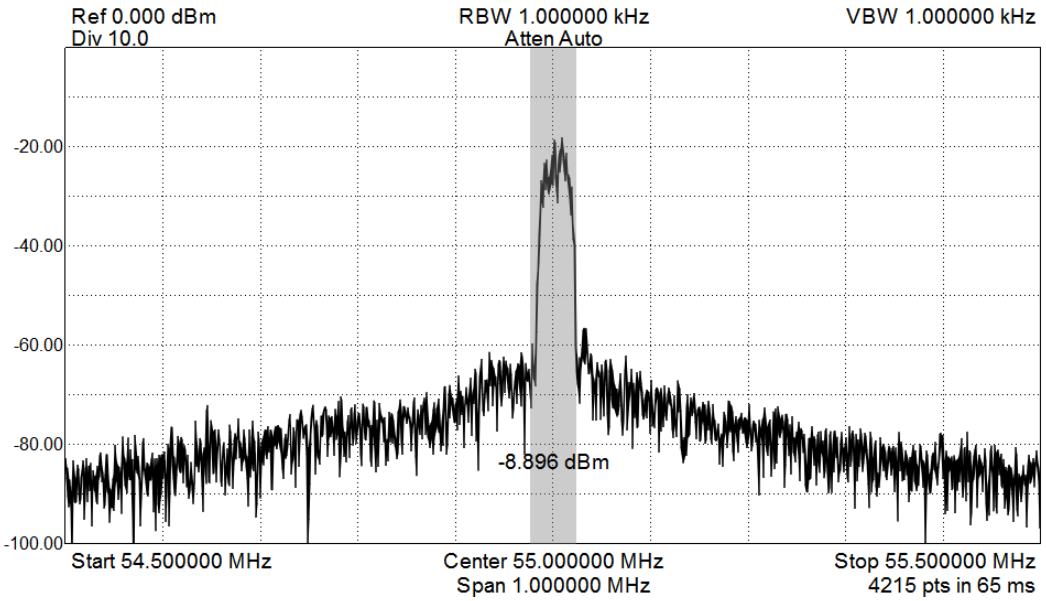

Figure 6.3: IF QPSK signal measure at the IFA output, with a system input attenuation of 50dB

These four point measurements were taken at a variety of input attenuation levels and the CNR calculated as shown above in equation 6.2.1. No odd behavior was seen at the LNA or mixer outputs across the applied attenuation

range. The overall input CNR versus CNR experienced at the output of the IFA amplifier is shown below in figure 6.4. The

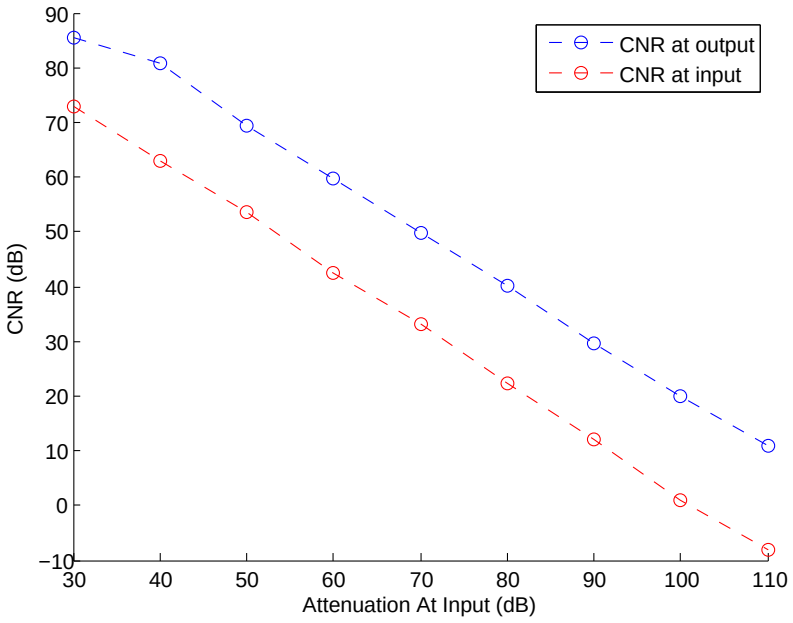

Figure 6.4: Measured system CNR

From this graph we can see the CNR ratio remains fairly constant over the attenuation range used. Thus even though there is a known non ideal mixer implementation, the operation is at least linear.

The CNR measurements were not done further than the IF amplifier output, since it was not possible to reliably measure the CNR at the output of the automatic gain control amplifier in this system. The operation of this component is however reflected in transceiver analysis in section 6.3.

6.3 Transceiver Performance

The overall transceiver performance was tested and validated by Hendrik Van Wyk. An in depth study of the communication protocol and back end system used for the system validation can be found in his thesis document, "Design and Construction of a Modem for Satellite Use". For the purpose of the research done during this project, we are interested in the final performance of the overall system.

6.3.1 Method of Evaluation

The two constructed transceivers were connected to two Linux based computers via the Ztek usb-xmega devices, each running the back end communication software designed by Van Wyk. The four patch antennas making up the two RF links were spaced evenly apart at 20cm. Since the the transceivers were designed for satellite communication but the test setup was at 20cm, attenuation was added until the system was not saturated.

The RF communication chain used for the BER testing was set up as half duplex, thus one radio acted as the receiver and the other as the transmitter. Once the system was in its operation phase in terms of received power, data throughput (BER for various levels of E_b/N_o) was measured. This was done by transmitting data packets at the specified baud rate. Attenuation was then increased several times, again measuring the effective data throughput for each attenuation value.

6.3.2 Overall Performance

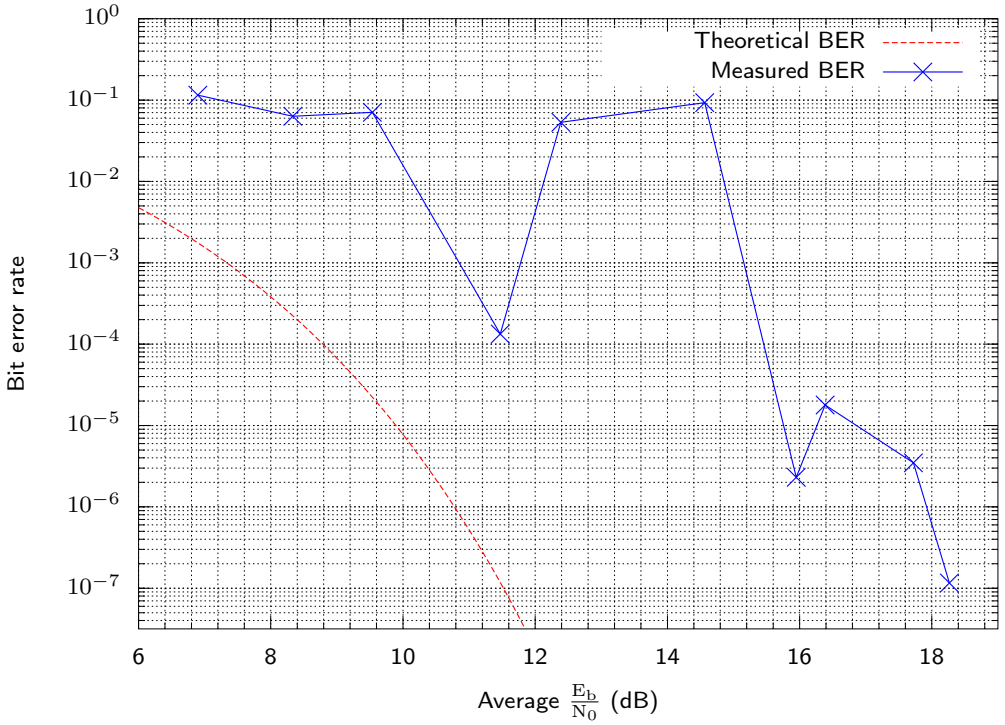

Figure 6.5: Bit Error Rate of the system using RF transmission and reception

Shown above in figure 6.5 is the Eb/No vs BER results of the testing done by Van Wyk. Shown in this graph is the measured system performance versus

the theoretical BER for BPSK communication.

6.3.3 Analysis of Results

From information received regarding the test setup, we know the following:

- All systems were connected correctly and powered accordingly.
- Attenuation was added at the transmission end to emulate a large free space loss.
- This attenuation was increased until the final amplifier input was not over saturated.
- The effective BER measurements were done at this level of attenuation.
- The attenuation was then increased and BER measured.
- This process was repeated until the AGC amplifier was at its maximum gain and beyond, until communication stopped being viable.

To draw a comparison between the tested system and it's theoretical performance, we need to compare the measured Eb/No vs BER ratios with theoretical values for the specific system. With the test setup explained above, let us first look at the received power.

Received Power

From the test parameters, we can assume that the AGC amplifier is not saturated and that it is operating correctly, keeping the output signal constant. In this range of operation, the AGC keeps the output voltage at $1V_{p-p}$. We can calculate the average amplifier power output using equation 2.3.17 as :

$$P_{avg} = \frac{0.5^2}{400} = 0.625\ mW \tag{6.3.1}$$

The output of this amplifier is matched at 50Ω, thus with no loss due to impedance mismatch, we can convert the output to dB, as shown below:

$$P_{avg} = 0.625mW = -32.04\ dB \tag{6.3.2}$$

This is the power supplied to the I/Q demodulator. To calculate the power supplied to its I and Q ports, we need to take it's conversion loss into account. P_I and P_Q can be calculated as :

$$P_I + P_Q = P_{avg} - L_{conv} = -32.04 - 5.3 = -37.34\ dB \tag{6.3.3}$$

Thus we know that the power at the I and Q ports combined equates to -37.34 dB. Since this power is split equally between the two ports, we know P_I = P_Q = -40.34 dB.

The final component in the chain is a low pass filter which adds an additional 1.5 dB loss. This filter lowers the power delivered to the ADC from -40.34dB to -41.83 dB, or 64.61 uW. With this received power and a specified baud rate of 62.5 kbps, we can calculate the power in a single bit E_b using equation 2.3.9 as:

$$E_b = \frac{P_{avg}}{R_b} = \frac{64.61 \times 10^{-}6}{62500} = 1.0441 \times 10^{-9}\ W = 1.0441\ nW \tag{6.3.4}$$

The AGC amplifier has discrete steps of effective gain and will at a certain point reach it's maximum gain. For the purpose of this analysis we assume that the gain is continuous and that the amplifier does not reach it's maximum gain. Thus the energy contained in each bit stays constant for the varying levels of attenuation applied to the system.

Effect of AGC amplifier

Before we do the equivalent noise temperature calculations, we need to take the following into account :

- Since certain component parameters vary according to frequency, the equivalent noise temperature will vary for the two RF frequencies the system operates at.
- The AGC gain has an effect on the system gain and T_{eq} calculation.
- The AGC noise factor is dependent on its gain. Due to the switched attenuator network operation of the AGC, the noise factor is lower for a higher gain value. This curve can be found in the appendix, figure B.2.

With these factors taken into account, it's clear that we require the AGC amplifier gain and noise figure for it's range of gain settings. The T_{eq} equation requires noise temperature, not noise figure. This conversion was done using equation 2.3.21 in section 2.3.5, with the results shown below in table 6.1.

Note the gain range of -2.5 dB to 42.5 dB is scaled to -13.78 dB to 31.22 dB, due to the impedance mismatch.

With these AGC amplifier noise temperatures and correlating gain values we have all the information required to start calculating the receiver noise power.

Table 6.1: AD8367 Noise figure vs Effective gain in a 50Ω System

Attenuation Setting (dB)	NF (dB)	Noise Temp (K)	Gain (dB)	Gain
0	6.2	918.92	31.22	1324.34
-5	9	2013.55	26.22	418.79
-10	15	8880.61	21.22	132.43
-15	20	28710.00	16.22	41.88
-20	26	115161.08	11.22	13.24
-25	32	459329.03	6.22	4.19
-30	37	1453152.98	1.22	1.32
-35	43	5785970.71	-3.78	0.42
-40	48	18297472.99	-8.78	0.13
-45	52	45961612.58	-13.78	0.04

Noise Power

The receiver noise power, as shown in equation 2.3.18 in section 2, can be calculated as:

$$N_o = k\left(T_{eq} + T_{ant}\right) BG_{rec} \tag{6.3.5}$$

First let us address the values in this equation that are unaffected by the AGC amplifier. These parameters are :

- Boltzmann Constant k
- The system Bandwidth B, determined by the final LPF which has a 3dB cutoff frequency of 750 kHz.
- The antenna noise temperature T_{ant}, which is assumed to be 300 K.

The overall receiver gain G_{rec} is dependent on the AGC gain The system equivalent noise temperature T_{eq} is dependent on both the AGC amplifier gain and its noise figure. Thus G_{rec} and T_{eq} need to be calculated across the entire range of AGC amplifier gain settings.

Using the equivalent noise temperature equation 2.3.20 given in section 2.3,

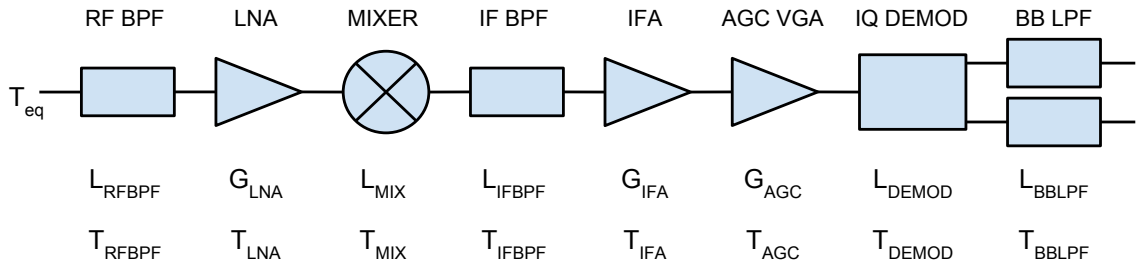

Figure 6.6: Receiver Layout

we can calculate theoretical equivalent noise temperature T_{eq} as:

$$T_{eq} = T_{RFBPF} + \frac{T_{LNA}}{G_{RFBPF}} + \frac{T_{MIX}}{G_{LNA}G_{RFBPF}} + \frac{T_{IFBPF}}{G_{LNA}G_{RFBPF}G_{MIX}} + \frac{T_{IFA}}{G_{LNA}G_{RFBPF}G_{MIX}G_{IFBPF}} + \frac{T_{AGC}}{G_{LNA}G_{RFBPF}G_{MIX}G_{IFBPF}G_{IFA}} + \frac{T_{DEMOD}}{G_{LNA}G_{RFBPF}G_{MIX}G_{IFBPF}G_{IFA}G_{AGC}} + \frac{T_{LPF}}{G_{LNA}G_{RFBPF}G_{MIX}G_{IFBPF}G_{IFA}G_{AGC}G_{DEMOD}} \tag{6.3.6}$$

Using equation 6.3.6 above, the component specifications shown in tables B.1 and B.2, and the AGC amplifier performance shown above in table 6.1, we can calculate the equivalent noise temperature T_{eq} for the full range of AGC amplifier gains. The results are shown below in table 6.2.

The final parameter required to calculate the receiver noise power is the receiver gain factor, G_{rec}, which is calculated as :

$$G_{rec} = L_{RFBPF} + G_{LNA} + L_{MIX} + L_{IFBPF} + G_{IFA} + G_{AGC} + L_{DEMOD} + L_{BBLPF} \tag{6.3.7}$$

By using the component specifications shown in tables 6.1,B.1 and B.2, we can calculate the range of G_{rec}, shown below in table 6.3.

Having characterized the effect of the variable AGC amplifiers effect on both the receiver gain G_{rec} and the equivalent noise temperature T_{eq}, we can now calculate the noise power for the transceiver at it's two operation frequencies. These N_o values for the range of amplifier gains are shown below in table 6.4

With the noise power (N_o) values for the variation in the AGC gain value and the received energy per bit (E_b) value calculated in equation 6.3.4, we can

Table 6.2: Equivalent Receiver Noise Temperature T_{eq} in K for both frequencies of operation (1.9GHz and 2.3GHz)

AGC Amplifier Gain (dB)	T_{eq} @ 1.9 GHz	T_{eq} @ 2.3 GHz
31.22	337.66	527.03
26.22	338.26	527.99
21.22	342.02	533.94
16.22	352.87	551.15
11.22	400.19	626.15
6.22	588.56	924.69
1.22	1132.51	1786.78
-3.78	3503.61	5544.73
-8.78	10350.70	16396.64
-13.78	25493.23	40395.93

Table 6.3: Receiver Gain Factor G_{rec} for both frequencies of operation (1.9GHz and 2.3GHz)

AGC amplifier gain (dB)	G_{rec} @ 1.9GHz	G_{rec} @ 2.3GHz
31.22	57.04	55.04
26.22	52.04	50.04
21.22	47.04	45.04
16.22	42.04	40.04
11.22	37.04	35.04
6.22	32.04	30.04
1.22	27.04	25.04
-3.78	22.04	20.04
-8.78	17.04	15.04
-13.78	12.04	10.04

calculate the Eb / No ratios. Then, using the BER equation 2.3.8, we calculate the theoretical BER for these Eb / No values. With these values we can compare the theoretical performance of the system with the results Hendrik van Wyk achieved. The theoretical Eb/No vs BER and a fitted version of the measured Eb / No values are shown below in figure 6.7.

Unmeasurable Negative Effects on System Performance

In figure 6.7 we can clearly see the difference in the performance achieved vs the theoretical data throughput. This difference in performance, also known

Table 6.4: Received Noise Power N_o and factors that contribute to it's calculations

1.9GHz RF Transmission			2.3GHz RF Transmission		
G_{rec} (dB)	T_{sys} K	No (pW)	G_{rec} (dB)	T_{sys} (K)	No (pW)
54.64	667.83	2012.83	52.64	813.42	1992.77
49.64	668.87	637.51	47.64	814.70	631.16
44.64	675.40	203.57	42.64	822.74	201.56
39.64	694.27	66.17	37.64	845.95	65.54
34.64	776.50	23.40	32.64	947.12	23.20
29.64	1103.84	10.52	27.64	1349.83	10.46
24.64	2049.11	6.18	22.64	2512.77	6.16
19.64	6169.61	5.88	17.64	7582.10	5.87
14.64	18068.50	5.45	12.64	22220.92	5.44
9.64	44383.20	4.23	7.64	54595.08	4.23

as implementation loss, can be attributed to the following unmeasured losses and effects :

- Noise temperature assumptions - Calculations were done assuming 300K room temperature. The actual temperature experienced during testing is unknown.
- Connector losses - These losses were compensated for in the individual component measurements, but the exact extent of this effect on the overall system performance is unmeasurable. Furthermore, each connector brings the possibility of adding additional impedance mismatches. The reflected waves caused by these impedance mismatches can have detrimental effect on the overall system performance, as well as reducing the effective power transmitted to the next component in the signal chain.
- Voltage Supply Noise - Care was taken to filter power supply lines and add decoupling capacitors where applicable. Unfortunately due to the mechanical layout of the transceiver components were spaced large distances from one another. This meant that power lines were long, and prone to picking up additional noise.
- Oscillator Noise - Even though the measured oscillator phase noise was relatively low, this does increase the overall system noise.
- Mixing Image Frequency Loss - Due to the nature of mixers, power is lost due to unwanted mixing images.

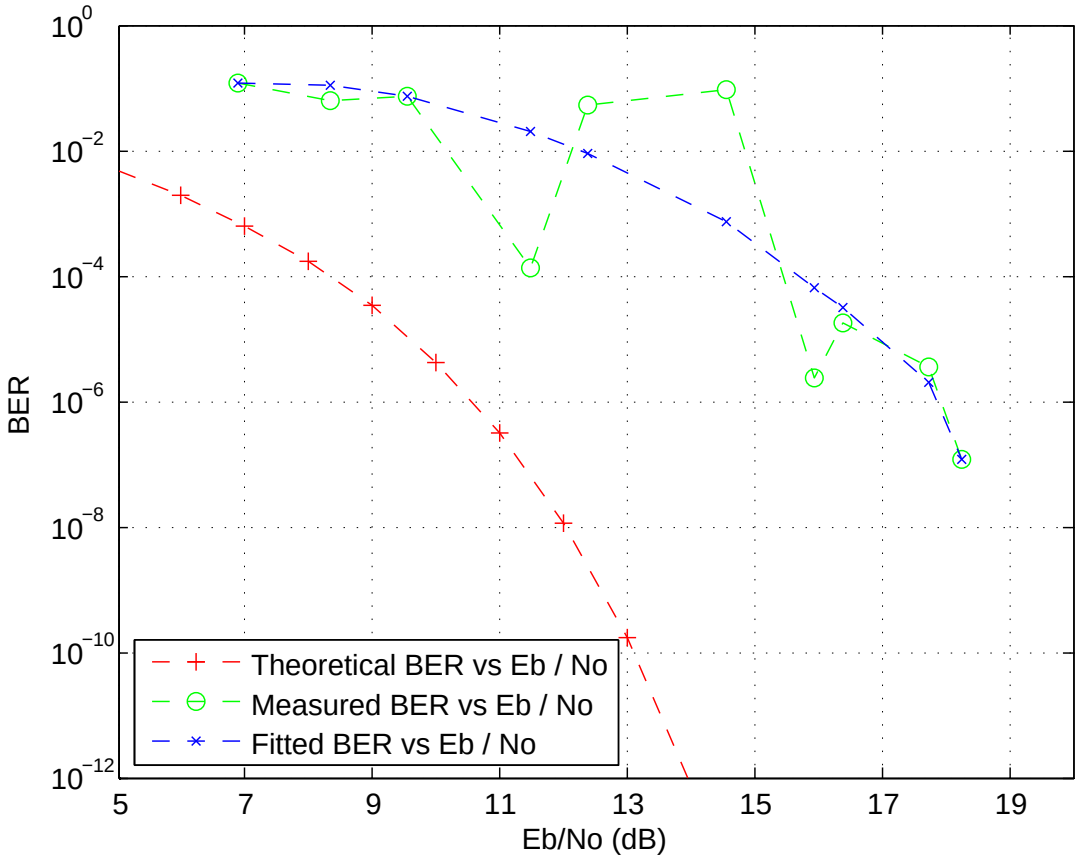

Figure 6.7: Comparison between theoretical BER vs Measured BER

- Uncertain placement of testing attenuators - The placement of the FSL imitation attenuators were not all placed at the transmission side of the transceiver. This could further increase the implementation loss.
- EMI - Electromagnetic interference due to other radiation sources not controlled during testing, further increases the system noise.
- Oscillator drift - Even though the PLL oscillators used had very good stability, there is drift due to varying operational conditions. The superhetrodyne transceiver layout used is even more sensitive to this phenomena, due to the amount of oscillators required.

Known Issues and Negative Effects on System Performance

Seen in figure 6.7, there are rather large discrepancies in terms of expected performance vs delivered performance. Except for the reasons of additional noise and power lost explained above, there is an additional effect induced during testing which we need to take into account. Once the transmitted

signal was attenuated enough not to saturate the receiver, Van Wyk started adding 1 dB attenuators to decrease the transmitted power even further.

Even though this methodology is sound, the AGC amplifier could not act correctly to each attenuator added, since the gain can only be varied in discrete steps of 5 dB. These discrete steps in gain, coupled with the addition of 1 dB attenuators, mean that under the worst case boundary condition, the signal could be amplified 4 dB less than used in calculations. (This does not take impedance matching into account) This is of course contrary to the assumption used to calculate the E_b value in equation 6.3.4. Thus this phenomena could be the reason the BER vs Eb/ No measured has sporadic upward jumps, instead of a constant decay.

Furthermore, the power distribution method described in chapter 5.11,which was used in the bench top version of the transceiver, was not ideal. Locating all power conditioning circuitry on a single PCB resulted in an architecture that more closely resembles that of an actual satellite transceiver, but for these tests it was not necessary. Lower noise and a more flexible test setup would have been possible if each component of the transceiver had it's own LDO and power filtering components. This single power conditioning PCB also heated up over longer periods of use. This increase in temperature experienced in longer duration tests had the effect of elevating the entire transceiver noise level.

Lastly, a mistake was made during the system layout phase of development. A RF band pass filter was placed between the antenna and LNA of both transceivers. This incorrect placement reduced the maximum data rate achievable with the developed hardware. It is also important to note that matched antennas used already greatly reduced the effect and necessity of these filters.

Unfortunately this error was only realised during the documentation of the project, and testing was already finalised. To quantify the magnitude of this error, we must look the impact the filter has on the receiver equivalent noise temperature T_{eq}.

Re-evaluating the equivalent system noise temperature show in equation

6.3.6 without the BPF the the input, we get :

$$T_{eq} = T_{LNA} + \frac{T_{MIX}}{G_{LNA}} + \frac{T_{IFBPF}}{G_{LNA}G_{MIX}} + \frac{T_{IFA}}{G_{LNA}G_{MIX}G_{IFBPF}} + \frac{T_{AGC}}{G_{LNA}G_{MIX}G_{IFBPF}G_{IFA}} + \frac{T_{DEMOD}}{G_{LNA}G_{MIX}G_{IFBPF}G_{IFA}G_{AGC}} + \frac{T_{BBLPF}}{G_{LNA}G_{MIX}G_{IFBPF}G_{IFA}G_{AGC}G_{DEMOD}} \tag{6.3.8}$$

Due to the concatenated nature of component noise and system noise calculations, the relatively low 1.8 dB loss induced by the BPF, has a substantial effect on noise temperature. To show this effect the incorrectly placed BPF had on the system, we will recalculate the T_{eq} using equation 6.3.8 for a single known AGC gain value and compare it with the T_{eq} value for the same AGC gain, taken from table 6.2. Using equation 6.3.8 and the same component specifications in tables B.1 and B.2, we can calculate the equivalent system temperature without the BPF at the LNA input T_{eq} as 167.65 K.

Thus the incorrectly placed PBF added 248 K to the overall system noise temperature on the 1.9 GHz link. Since this mistake was made on both communication links, we observe a substantial difference on the 2.3 GHz link as well, with the T_{eq} dropping with 288.12 K, from 527.47 K to 239.35 K.

Using this updated layout and the equivalent noise temperature equation 6.3.8, we can also observe which components have the largest effect on the overall system noise. This method of evaluation could identify further non ideal component choices. Taking the first term of equation 6.3.8 as the LNA noise contribution and term two as the mixer noise contribution and so forth, we can populate the following table of component noise contributions:

Table 6.5: Receiver chain component noise contributions @ 1.9 GHz

Component Name	Noise Temperature (K)	Contribution to T_{eq} (K)
LNA	50.72	50.72
Mixer	1000.5	44.9
IF BPF	35.39	7.06
IF Amp	288.6	64.65
AGC Amp	918.9	0.33

From table 6.5 we can clearly observe the concatenated nature of system noise temperature, since the effect of a components individual noise temperature becomes less the further down the communication chain its located. This is not the case with the IF amplifier, which makes it the first component that

would require re-evaluation.

6.4 Doppler Shift Compensation

To fully control all the variables that could affect the Doppler shift compensation circuit, it was not tested with the main transceiver described in section 6.3. Instead it was tested separately.

6.4.1 Method of Evaluation

To test the compensation circuit without adding any additional unexpected noise components, a QPSK modulated signal, generated by a Rhode and Schwarz vector signal generator, was applied to the circuit as an input. The selected baud rate was 48.2 kbps with a carrier frequency of 55 MHz. This carrier frequency was then varied to simulate the passing of a LEO satellite over a base station. One can clearly observe the unfiltered QPSK modulation in the spectrum seen in figure 6.9, with the baud rate of 48.2 clearly visibly in the oscilloscope plot in figure 6.8 below.

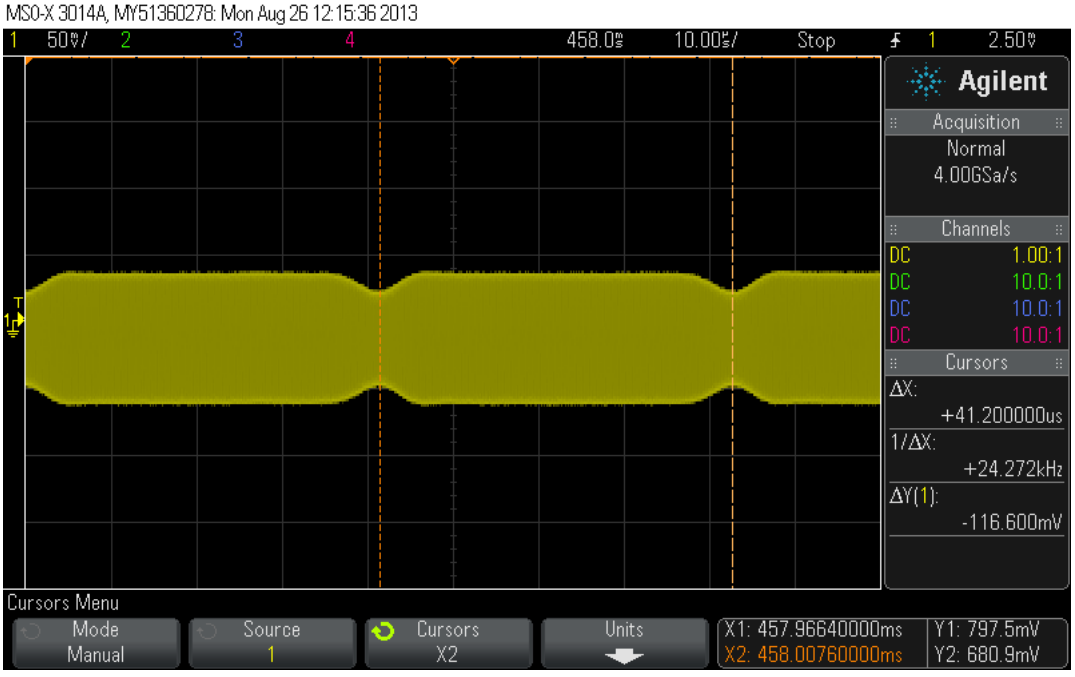

Figure 6.8: Oscilloscope screen capture of the unfiltered QPSK signal used to test the Doppler shift circuit

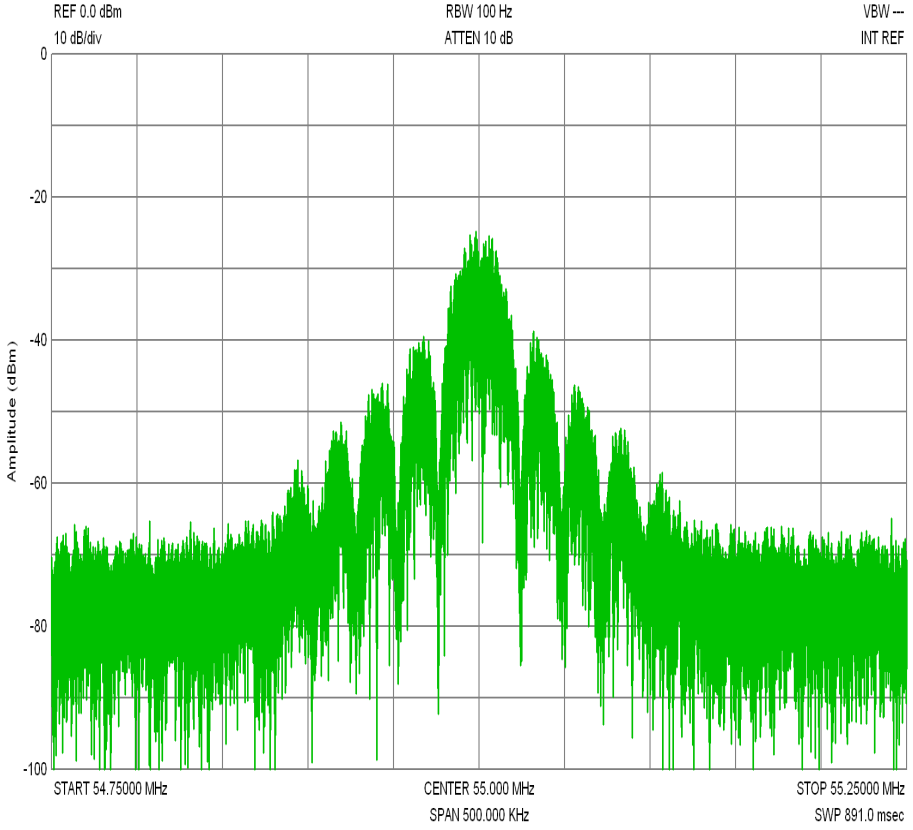

Figure 6.9: Spectrum analyzer capture of the 55Mhz unfiltered QPSK modulated signal used to test the Doppler shift circuit

6.4.2 Overall Performance

The unfiltered QPSK signal (shown above in figure 6.9) is applied to the Doppler shift compensation circuit. With this input signal, which has a correct carrier frequency of 55MHz, a unfiltered output shown in figure 6.10 is observed.

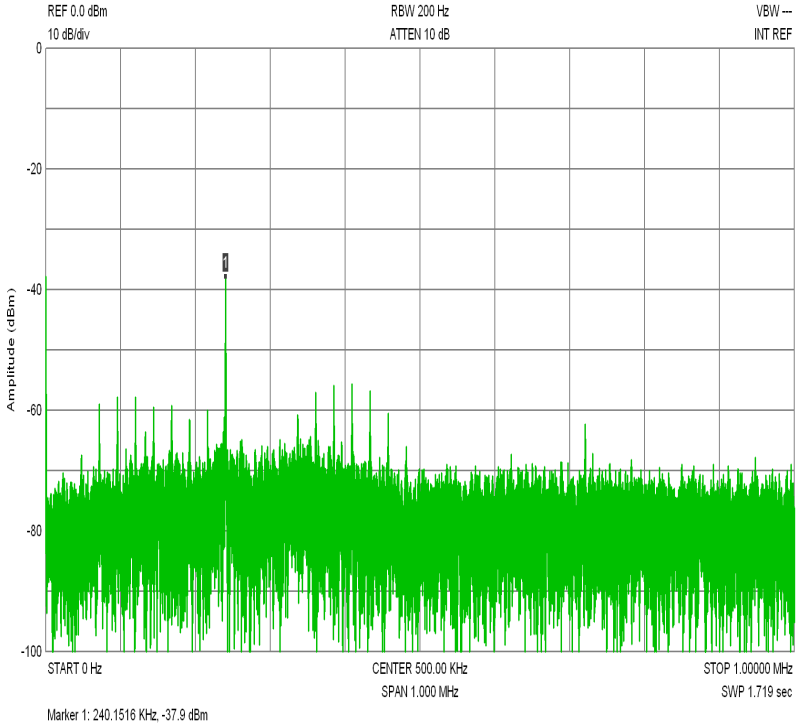

Figure 6.10: FFT of the Doppler shift extractor output with a unfiltered QPSK as system input

This output is then sent through the LPF and a voltage level converter to give the the oscilloscope output below in figure 6.11.

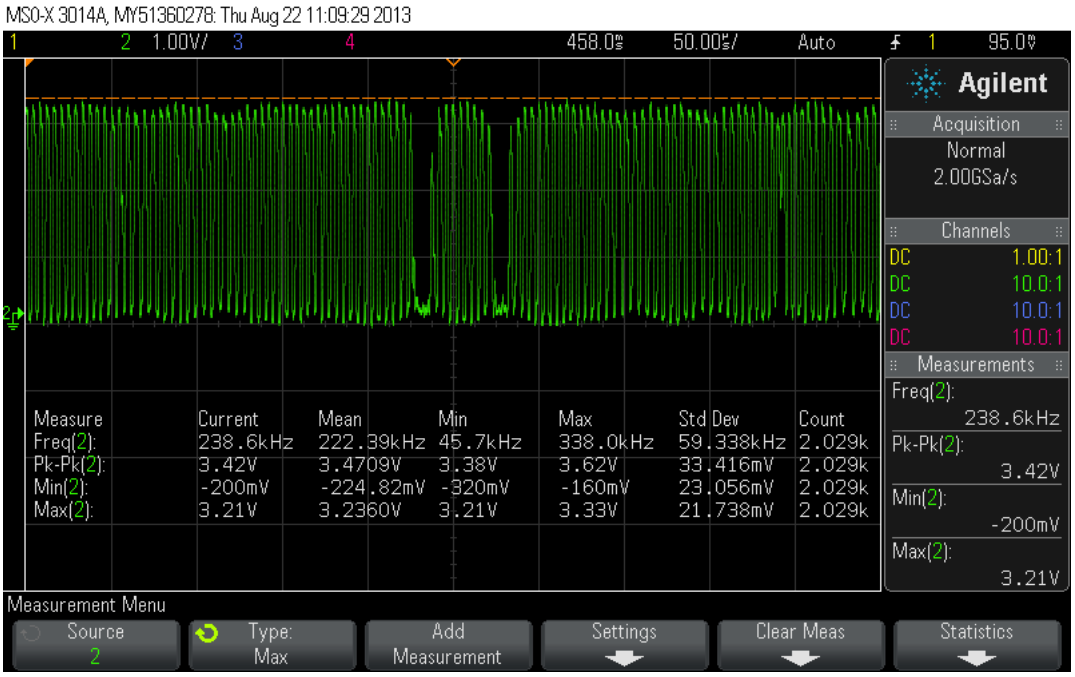

Figure 6.11: Oscilloscope screen shot of the Doppler shift extractor output

6.4.3 Analysis of Results

As explained in chapter 5.9, the system was designed to output 240kHz when no Doppler shift is experienced. This output frequency was clearly observed, and can be seen below in figure 6.11. Also clearly visible are dead times in the output signal. These are due to the phase modulation scheme used, and occurs when the phase of the signal is changed, at a rate of 24.1kHz. Using count averaging explained in section 5.10.2.1 we can compensate for this counted frequency deviation.

Adjusting the 55MHz carrier frequency simulated a Doppler shift in the received signal. This variation in input signal was clearly measurable on the micro controller, with an increased carrier frequency having a x4 effect on the counted signal measured. The same behavior was observed when decreasing the carrier frequency below 55MHz, simulating the satellite moving further away from the base station. This counted and averaged frequency deviation can then be used to re-program the LO used for demodulation, via SPI.

Considering that we could correctly extract the shift in carrier frequency of a supplied phase modulated signal, and adjust a demodulator oscillator to compensate for the experienced shift in carrier frequency, the Doppler shift compensation circuit worked as expected.

6.5 Brief Summary and Prognosis for Next Chapter

Both the transceiver and Doppler shift compensation circuit proved to be operational. In the next chapter we will take a critical look at these results to ensure that the project achieved the goals it originally set out to achieve.

Chapter 7

Conclusions and Recommendations for Further Work

7.1 Conclusions

Two S Band transceivers were designed and built. These superhertrodyne transceivers were built of modular components, and while attempting to use only off the shelf components, several parts of the transceiver required detailed electronic design and manufacturing. The completed two transceivers were successfully integrated with an associate project, which allowed the completed system to be fully tested. Testing showed satisfactory results. Experienced noise levels were higher than the theoretically calculated values, which in turn resulted in lower effective data rates. These effects were attributed to known mistakes in the chosen design as well as unexpected or unmeasurable effects, commonly known as implementation loss.

A methodology to compensate for the Doppler shift experienced in LEO satellite communication, by measuring the shift and adjusting the demodulation oscillator, was also designed and constructed. Using a vector signal analyzer as source, a QPSK signal was applied to the circuit with its carrier frequency varying in the same range a LEO satellite would experience while orbiting the earth. The deviation from the required carrier frequency could be correctly extracted and measured.

7.2 Outcomes

Upon completion of the project, the following outcomes were achieved:

- Thorough research done on the unique requirements of a telecommuni-

cation system in LEO satellites.

- Simulation software package developed to determine boundary conditions experienced in communication link quality.
- The design and development of a adjustable, wide band, oscilator.
- Successfully designed, constructed and tested two S Band transceivers which can serve as a working prototype for a high speed TT&C link.
- Integrated the designed transceivers with an associate project in the same area of study
- Successfully designed, constructed and tested a Doppler shift compensation circuit which operates by adjusting the demodulation oscillator, rather than compensating for the shift digitally.

7.3 Recommendations for Further Work

The modulation scheme implemented in the final version of the experimental TT&C link was BPSK. The modulation on baseband level is done with ADCs and DACs, which are connected to I&Q modulators and demodulators. Due to this modulation implementation, it would be easy to evaluate the performance of more complex M-ary modulation schemes, without any hardware modifications.

A thorough review of the implemented transceiver design, coupled with the optimization of critical parameters and replacing known non-ideal components, would generate a transceiver design perfectly suited for use as a modular S Band TT&C link.

Mixer Implementation

As described in relative detail in chapter 5.12.8, the RF mixer implemented in this project was not used under ideal circumstances. With the addition of impedance matching baluns or by selecting a mixer that is matched at the required frequencies, the overall system performance would be better.

AGC VGA impedance matching

Due to a technical oversight and limited time, the AGC VGA impedance matching was done with a voltage divider circuit. This is considered poor practice, since it hampers performance and decreases the amount of power that can be delivered to the rest of the system. An impedance matching guide can be found in the AD8367 data sheet. Replacing this inefficient resistor based

impedance matching scheme with the minimum-loss, L-pad network matching described in the data sheet, the overall system performance can be further increased.

7.4 Project Retrospective

A key part of learning and growing in a specific field is the ability to observe one's methods and actions in retrospect, and to ensure that one clearly understand the mistakes made. The focus of this section is to be critical of the work done and to illuminate where the the author made mistakes which could not be corrected for in the given timespan of this project.

Specification Orientated Design

This was to a large extent a co-development project between two students. At its conception the lines were slightly blurred surrounding who exactly would be responsible for defining what aspect of the overall system. No clear interface requirements were defined by either party. We worked next to one another, planning and exchanging ideas. Constantly changing the overall system design and performance, to suite our current train of thought. Building the system from it's basis to something that operates within the bounds of what one would find within the satellite industry. Unfortunately this approach left a lot to be desired in terms of comparing the achieved results with what the intended system performance should be. The lesson learned here is that it is very difficult to measure success of a design endeavor if one does not develop towards a clearly specified specification.

Outcome Based Development Approach

Without a fixed specification in place, the development and design process that was followed had very little structure. Instead of taking a systematic outcomes based approach, clearly understanding the effect each component would have on the final result, a far more ad-hoc process was used. This was in part due to the ever moving goal of the project. Parts, operating frequencies and requirements were constantly changed and adjusted, taking care to ensure that the overall system still functions, but disregarding a focused logical design process. As working towards a specification is a critical part of a project, properly defining the development process before hand is just as critical. The correct approach that should have been followed is : Define a overall system requirement, which in turn defines the individual component requirements. One would then design or acquire each component, ensuring that it adheres to these requirements. Testing is then done on a component level, ensuring it adheres to the requirements set. Only once this is done can the overall system be tested. These system wide results can be compared with the initial

system requirements, quantitatively measuring the success of the development process.

Best Practice Research

A lack of experience and a determined can-do attitude did far more harm than the author intended. Having done countless small projects wherein the final result was binary, i.e. it either works or it doesn't, shaped the authors methodology in approaching this project. When an issue arose the author used the skills and knowledge to address the issue as quickly as possible. More research into industry accepted best practice techniques before addressing an issue would have solved several issues experienced in this project. A key example of this is the unmatched mixers used. Using a component with a non ideal VSWR at such a critical point in a receiver is unheard of in industry applications. Instead of doing in depth research at the time, the author selected a component with an acceptable input and output frequency range, and moved his focus onto the next component in the signal chain.

Result Focused Research

This is a relatively minor realization, but important none the less. A lot of work was done by the author that had no place in this document. Work that has no place in the success of the project, but was important for the author. For instance, a massive amount of time was spent on understanding how the analog Devices VCO / PLL operates, since it was a extremely versatile and fascinating component. Was this in depth understanding necessary for the success of the overall project? No. Implementing the recommended registry setup in the data sheet would have sufficed. Similarly, the author taught himself to solder and crimp high frequency SMA cables, since it's a skill he wanted to learn at the time. Was it necessary for the success of the project? No, he could have used the university support system to order cables to specification. Even though the author does not regret the decision to spend time acquiring these skills and knowledge, a key lesson learned here is that in a time critical project such as a masters thesis, one should ensure that the time spent on research is towards the project goal and not that of the author. In future projects a more balanced approach to personal enrichment and project success would be pursued.

Appendices

Appendix A

Test Results

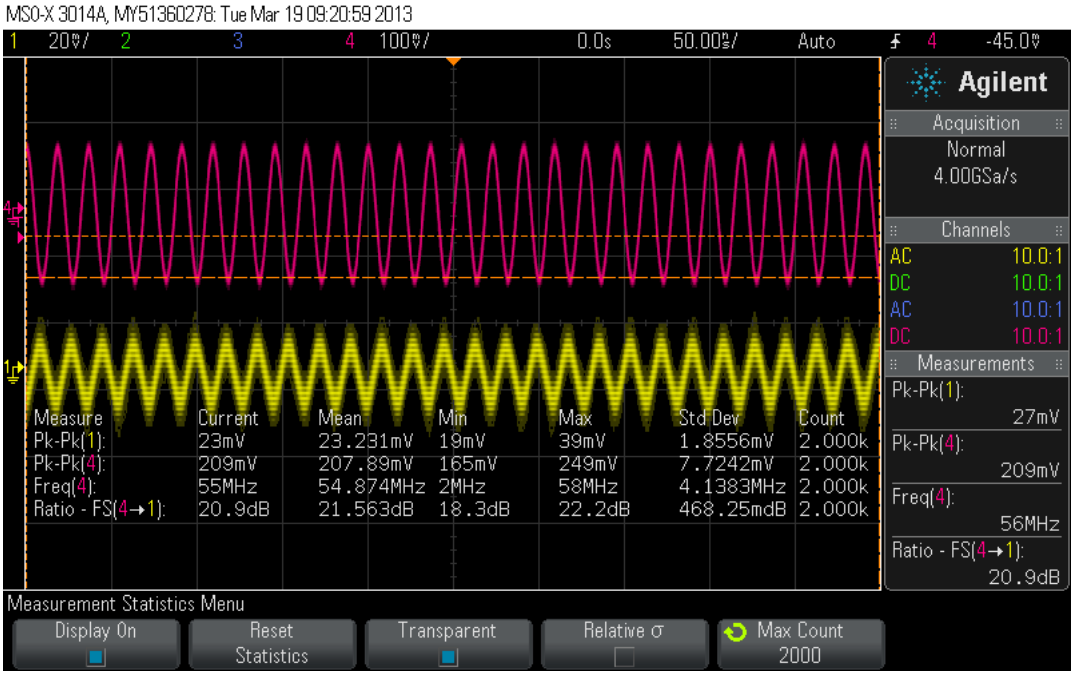

Figure A.1: Ad83267 Input vs Output signals @ 55MHz

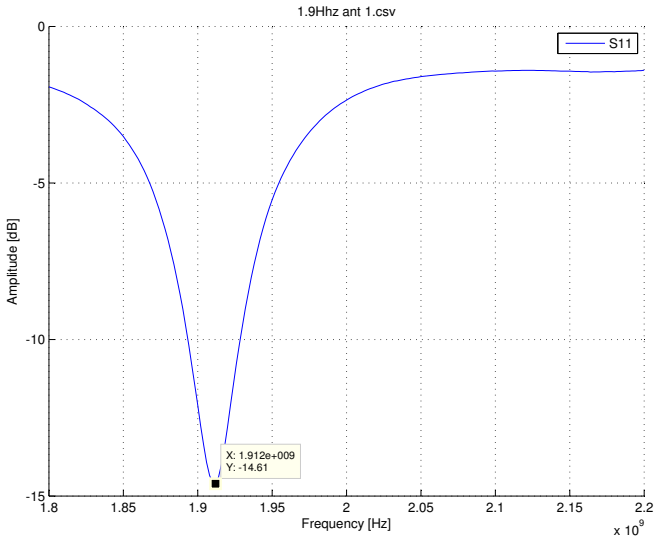

Figure A.2: First 1.9GHz Patch Antenna S_{11} Parameters measured with a Vector Analyzer

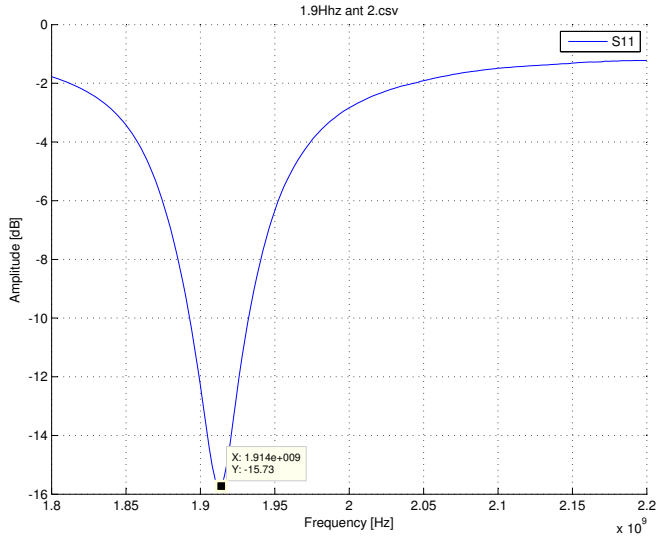

Figure A.3: Second 1.9GHz Patch Antenna S_{11} Parameters measured with a Vector Analyzer

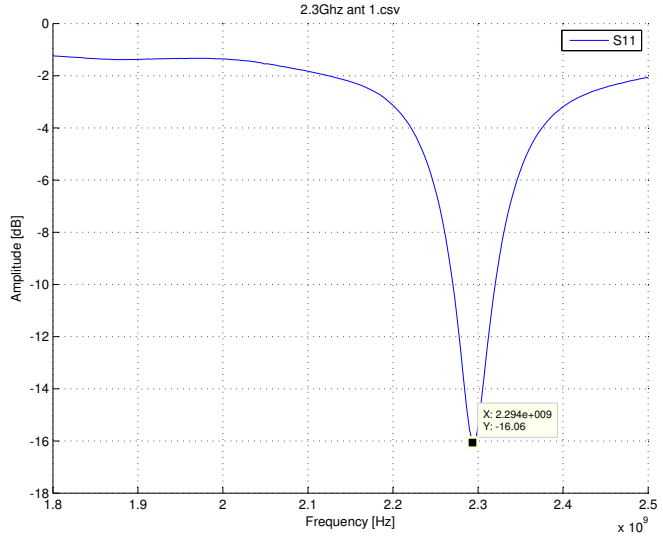

Figure A.4: First 2,3GHz Patch Antenna S_{11} Parameters measured with a Vector Analyzer

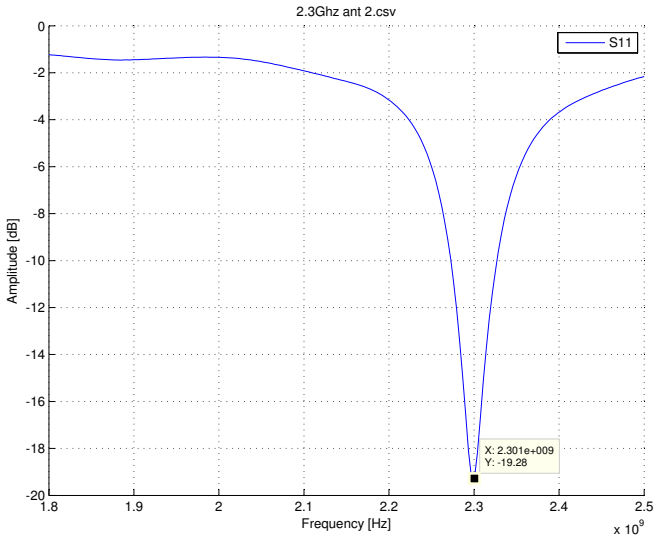

Figure A.5: Second 2,3GHz Patch Antenna S_{11} Parameters measured with a Vector Analyzer

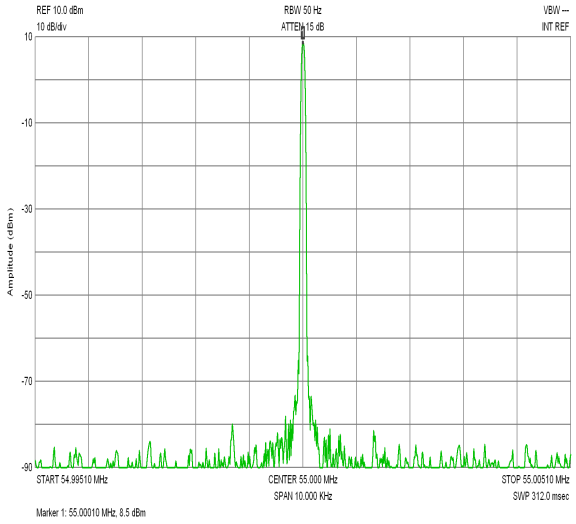

Figure A.6: ADL4351 Operating at 55MHz Amplitude Measurement

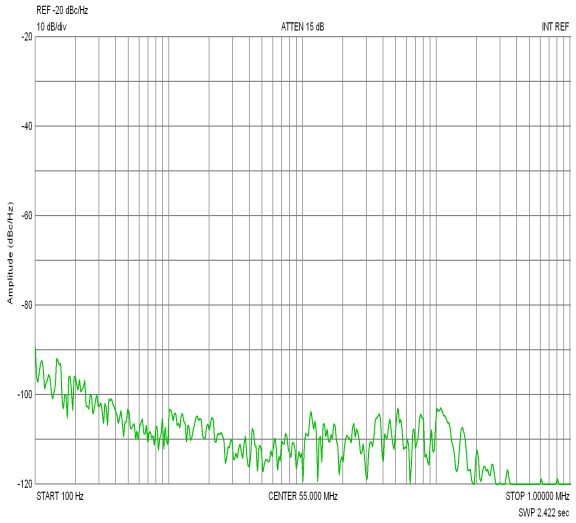

Figure A.7: ADL4351 Operating at 55MHz Phase Noise Measurement

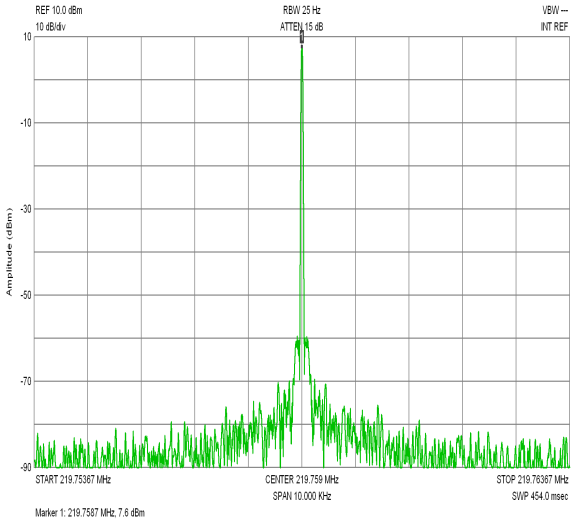

Figure A.8: ADL4351 Operating at 219.76MHz Amplitude Measurement

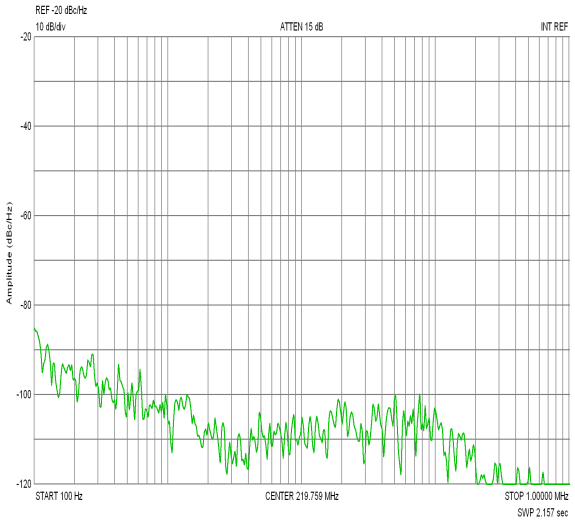

Figure A.9: ADL4351 Operating at219.76MHz Phase Noise Measurement

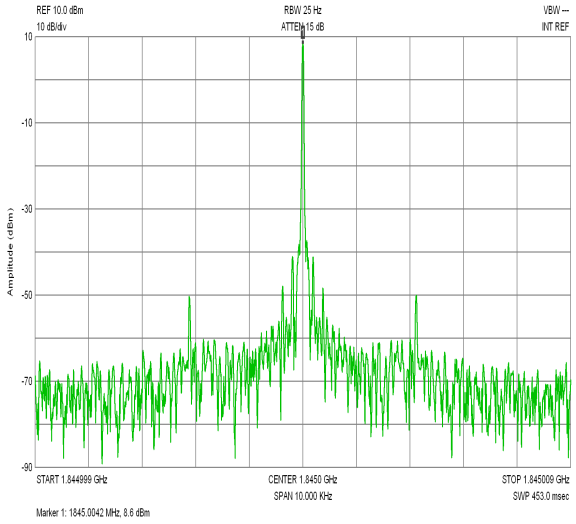

Figure A.10: ADL4351 Operating at 1.845GHz Amplitude Measurement

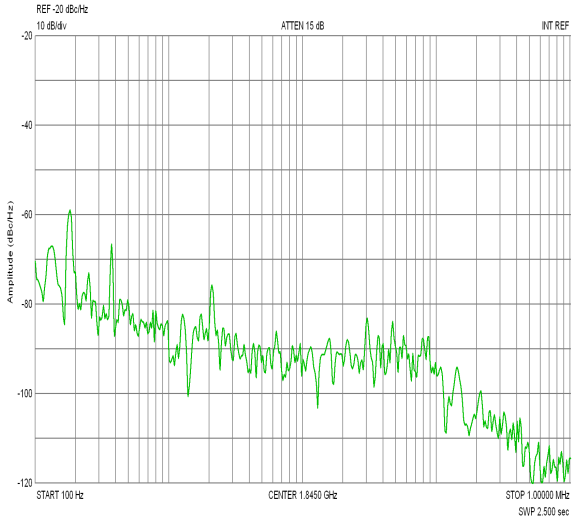

Figure A.11: ADL4351 Operating at 1.845GHz Phase Noise Measurement

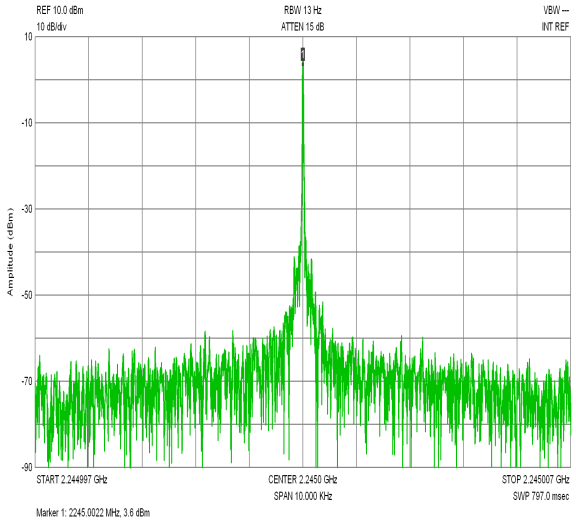

Figure A.12: ADL4351 Operating at 2.245GHz Amplitude Measurement

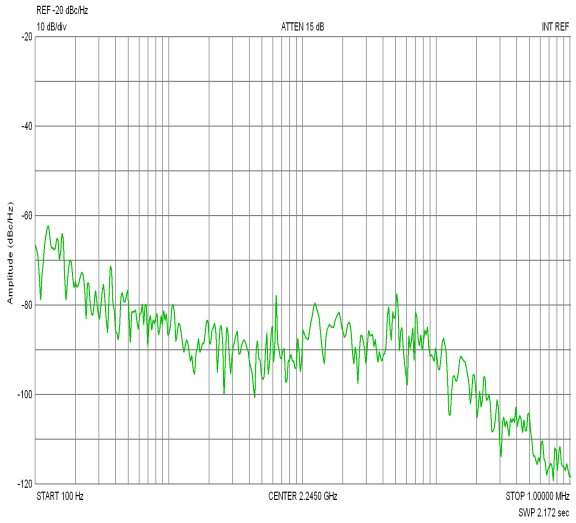

Figure A.13: ADL4351 Operating at 2.245GHz Phase Noise Measurement

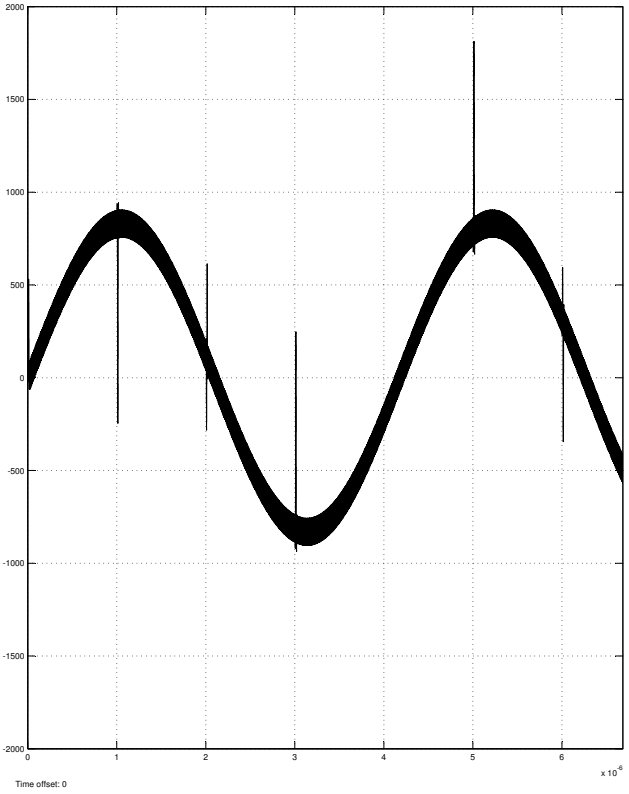

Figure A.14: Matlab Simulink output of 240kHz with a original carrier frequency of 55MHz

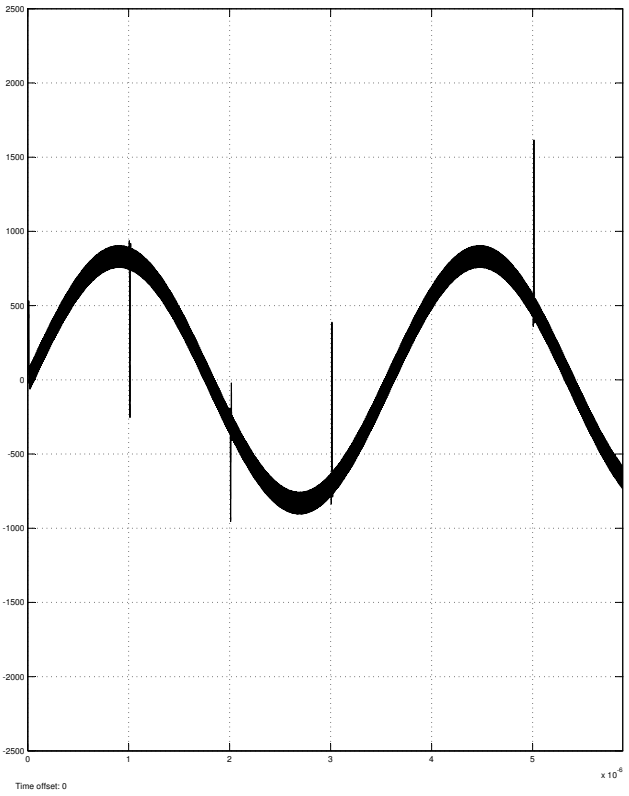

Figure A.15: Matlab Simulink output of 280kHz with a original carrier frequency of 55.01MHz

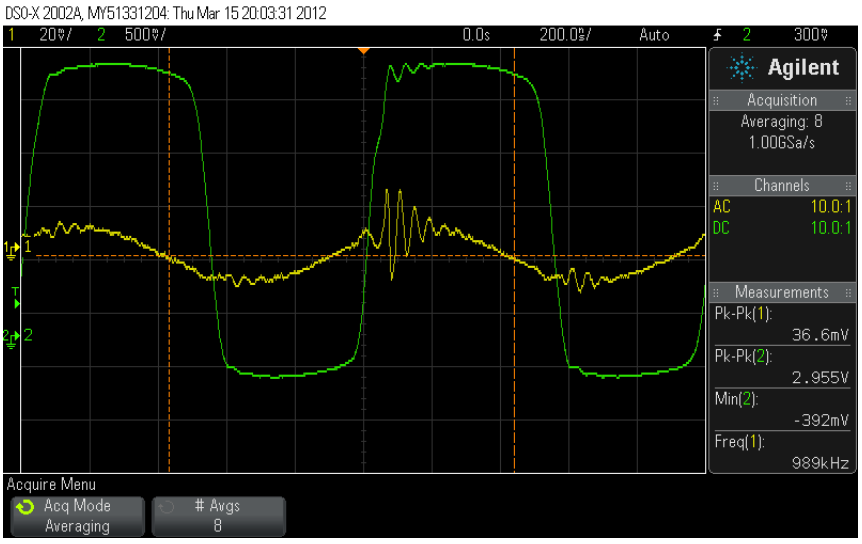

Figure A.16: Input and output of the comparator circuit used in the Doppler shift extractor

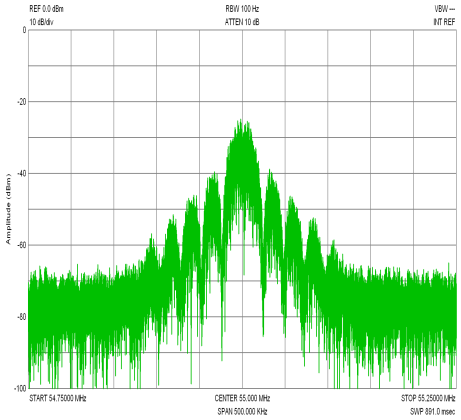

Figure A.17: FFT of the 55MHz Unfiltered QPSK input signal used for Doppler shift extraction tests

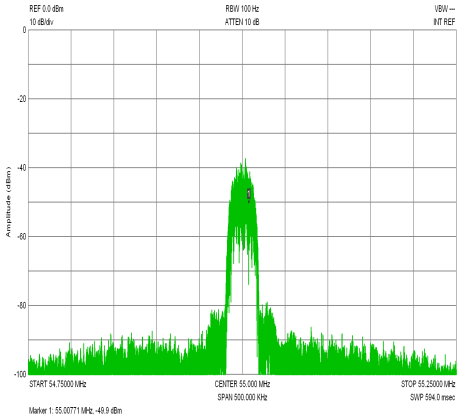

Figure A.18: FFT of the 55MHz Filtered QPSK input signal used for Doppler shift extraction tests

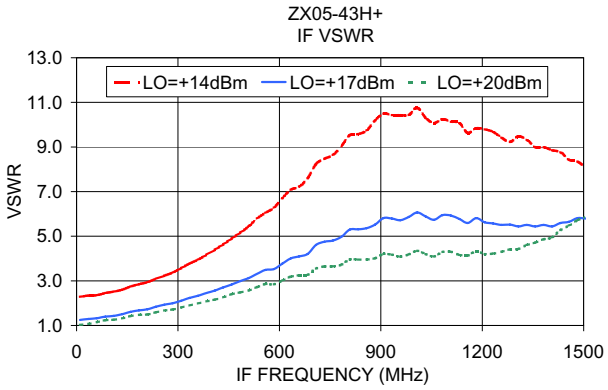

Figure A.19: IF VSWR of ZX05-43H+ Mixer [6]

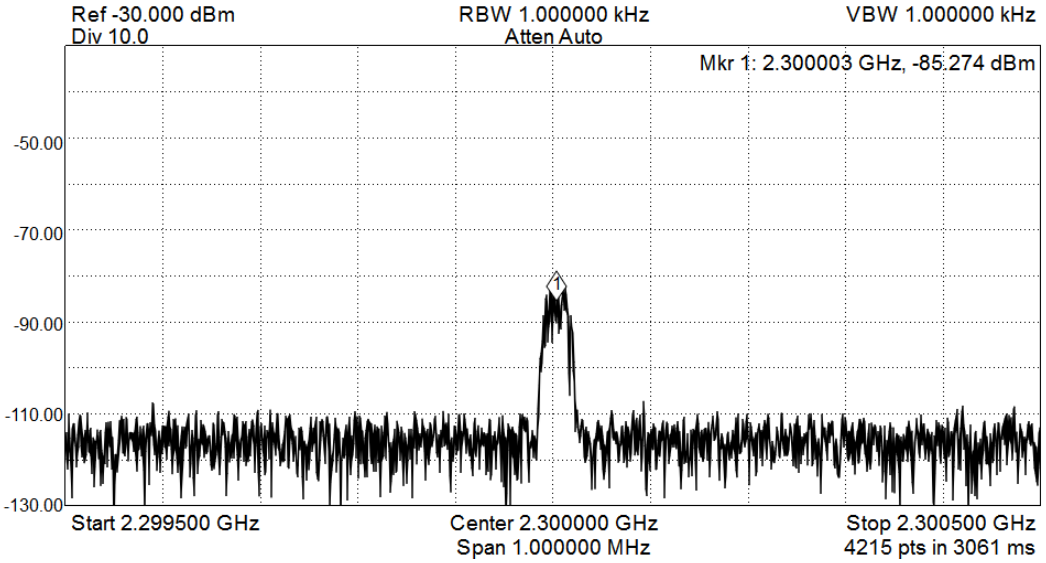

Figure A.20: LNA test at 2.3GHz input FFT

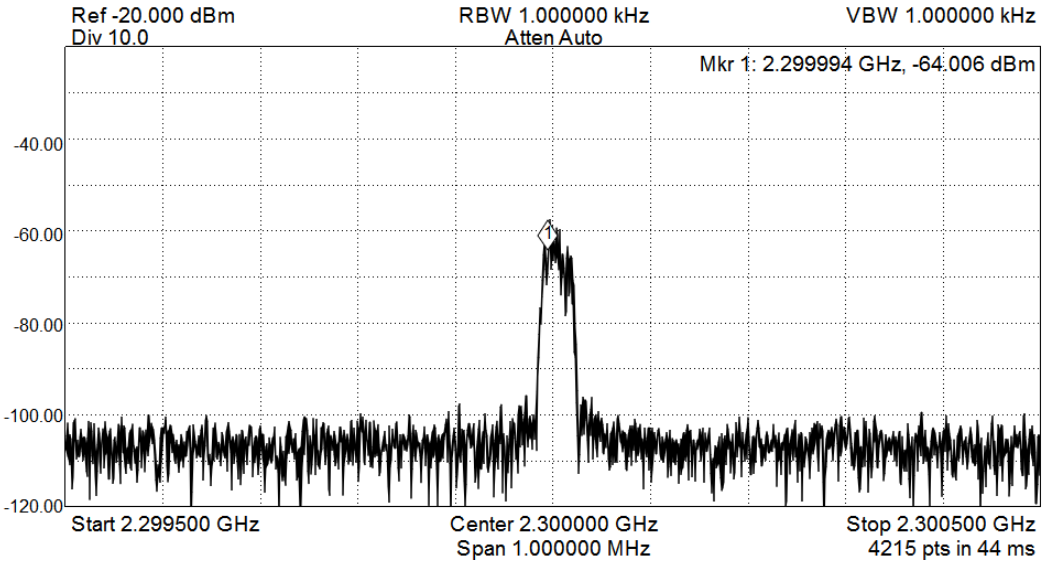

Figure A.21: LNA test at 2.3GHz output FFT

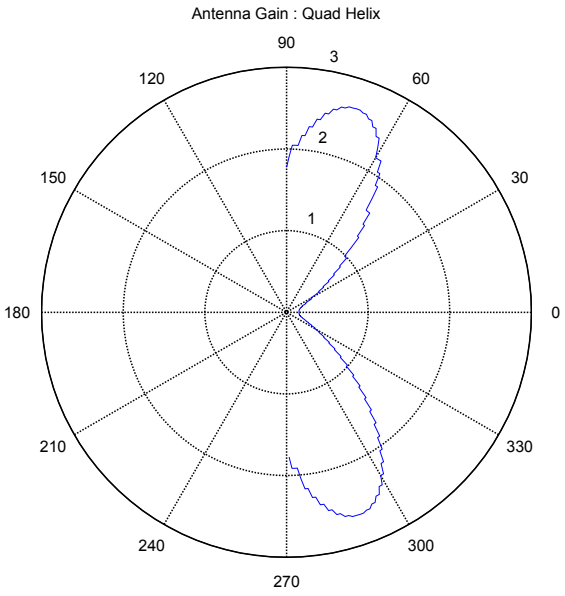

Figure A.22: Polar graph plot of a Quadrifilar helix antenna EIRP generated by SatSim

Appendix B

Data sheet extracts

B.1 Component Specifications

Table B.1: LNA Gain and Noise parameters for the two frequencies of operation

Parameter	Value at 1.9GHz	Value at 2.3GHz
NF_{LNA}	0.7dB	0.75dB
T_{LNA}	50.72K	54.67K
G_{LNA} dB	13.5dB	11.5dB
G_{LNA}	22.39	14.13

REGISTER MAPS

REGISTER 0

RESERVED	16-BIT INTEGER VALUE (INT)																12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED			PHASE ADJUST	PRESCALER	12-BIT PHASE VALUE (PHASE) DBR[1]												12-BIT MODULUS VALUE (MOD) DBR[1]												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	PH1	PR1	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3(0)	C2(0)	C1(1)

REGISTER 2

RESERVED	LOW NOISE AND LOW SPUR MODES		MUXOUT			REFERENCE DOUBLER DBR[1]	DBR[1] RDIV2	10-BIT R COUNTER DBR[1]									DOUBLE BUFFER	CHARGE PUMP CURRENT SETTING DBR[1]				LDF	LDP	PD POLARITY	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L2	L1	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	CP4	CP3	CP2	CP1	U6	U5	U4	U3	U2	U1	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED								BAND SELECT CLOCK MODE	ABP	CHARGE CANCEL	RESERVED	CSR	RESERVED	CLK DIV MODE		12-BIT CLOCK DIVIDER VALUE												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	F4	F3	F2	0	0	F1	0	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED								FEEDBACK SELECT	DBB[2] RF DIVIDER SELECT			8-BIT BAND SELECT CLOCK DIVIDER VALUE								VCO POWER-DOWN	MTLD	AUX OUTPUT SELECT	AUX OUTPUT ENABLE	AUX OUTPUT POWER		RF OUTPUT ENABLE	OUTPUT POWER		CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	D13	D12	D11	D10	BS8	BS7	BS6	BS5	BS4	BS3	BS2	BS1	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(1)	C2(0)	C1(0)

REGISTER 5

RESERVED								LD PIN MODE		RESERVED	RESERVED		RESERVED																CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	D15	D14	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C3(1)	C2(0)	C1(1)

[1]DBR = DOUBLE-BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
[2]DBB = DOUBLE-BUFFERED BITS—BUFFERED BY THE WRITE TO REGISTER 0, IF AND ONLY IF DB13 OF REGISTER 2 IS HIGH.

09800-023

Figure 23. Register Summary

Figure B.1: ADF4351 register map

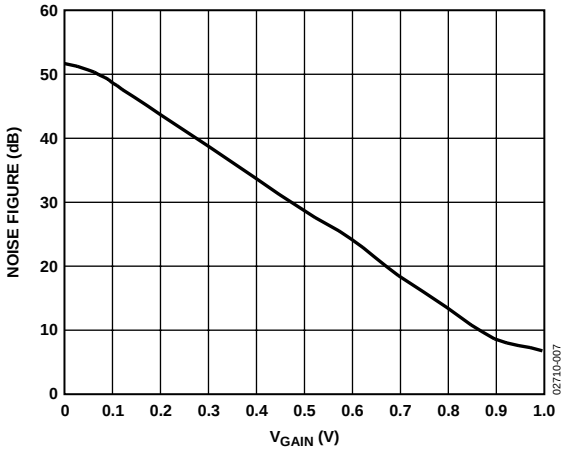

Figure B.2: AD8367 Noise Figure vs gain setting

Table B.2: Transceiver component gain and noise parameters

Parameter	Theoretical Value
NF_{RFBPF} dB	1.88dB
T_{RFBPF}	157.1K
L_{RFBPF} dB	1.88dB
L_{RFBPF}	1.543
G_{RFBPF}	0.648
NF_{MIX}	6.5dB
T_{MIX}	1000.5K
L_{MIX}dB	6.5dB
L_{MIX}	4.47
G_{MIX}	0.2237
NF_{IFBPF} dB	0.5dB
T_{IFBPF}	35.39K
L_{IFBPF} dB	0.5dB
L_{IFBPF}	1.12
G_{IFBPF}	0.8938
NF_{IF}	3dB
T_{IF}	288.6K
G_{IF}dB	28dB
G_{IF}	630.96
NF_{AGC}	6.2dB
T_{AGC}	918.9K
G_{AGC}dB	30dB
G_{AGC}	1000

Appendix C

Schematics and PCB Layouts

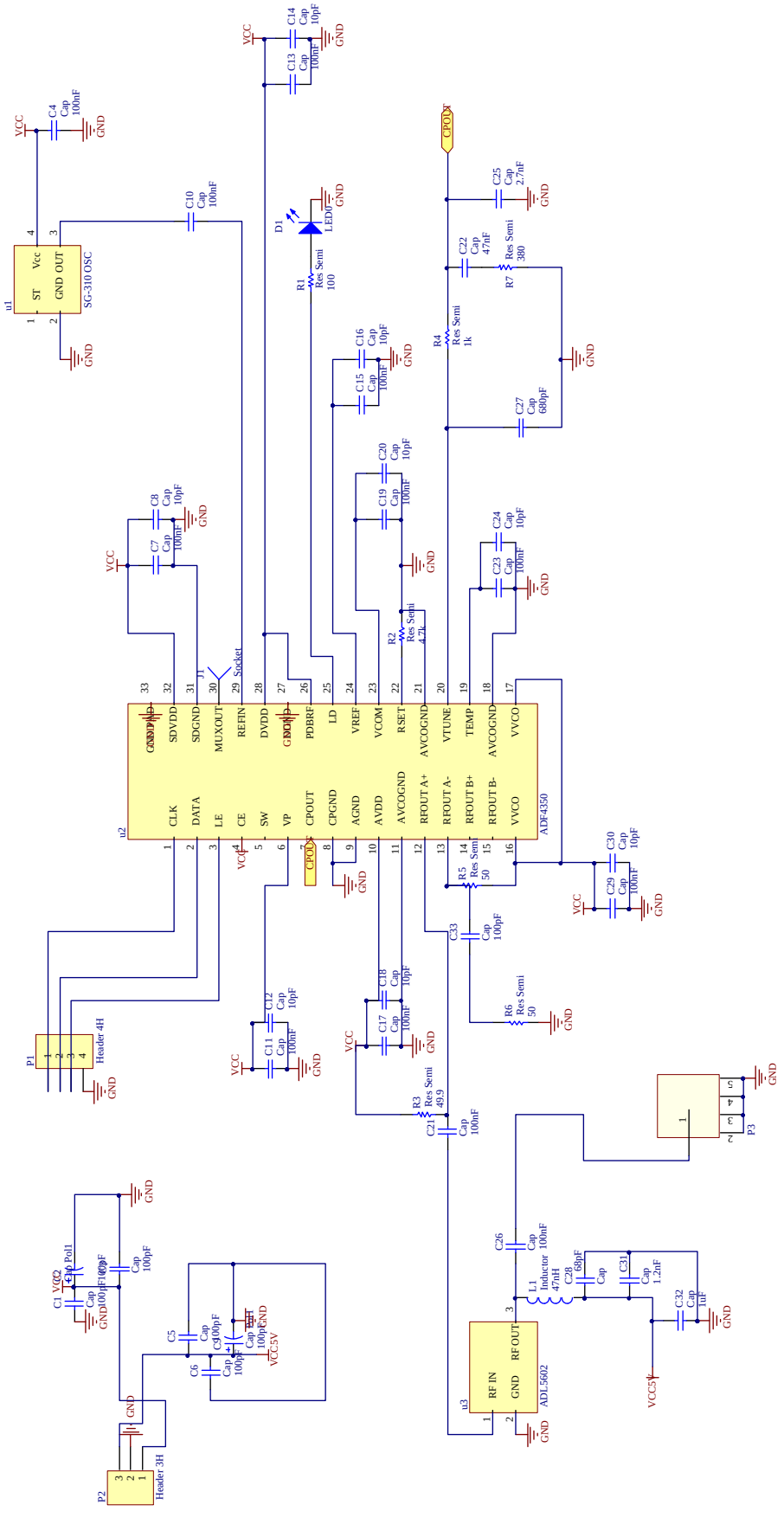

Figure C.1: ADF4351 Schematic

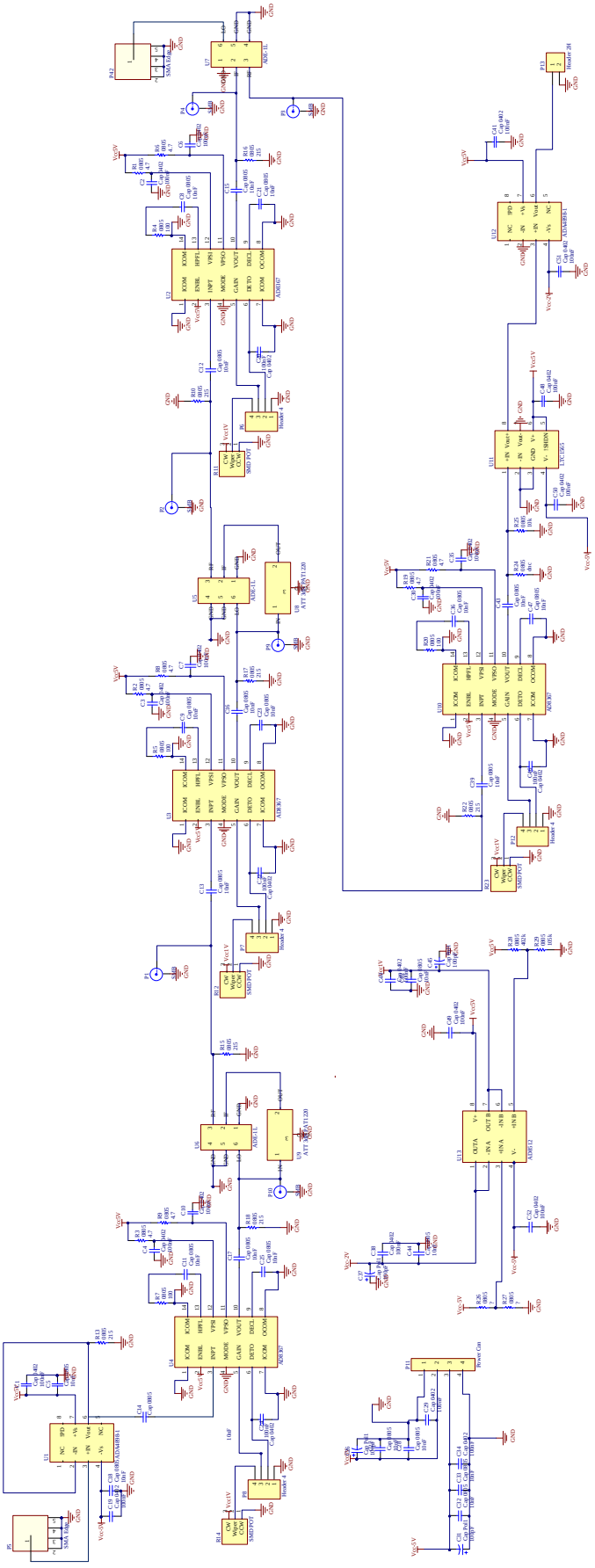

Figure C.2: Doppler Shift Compensator Schematic

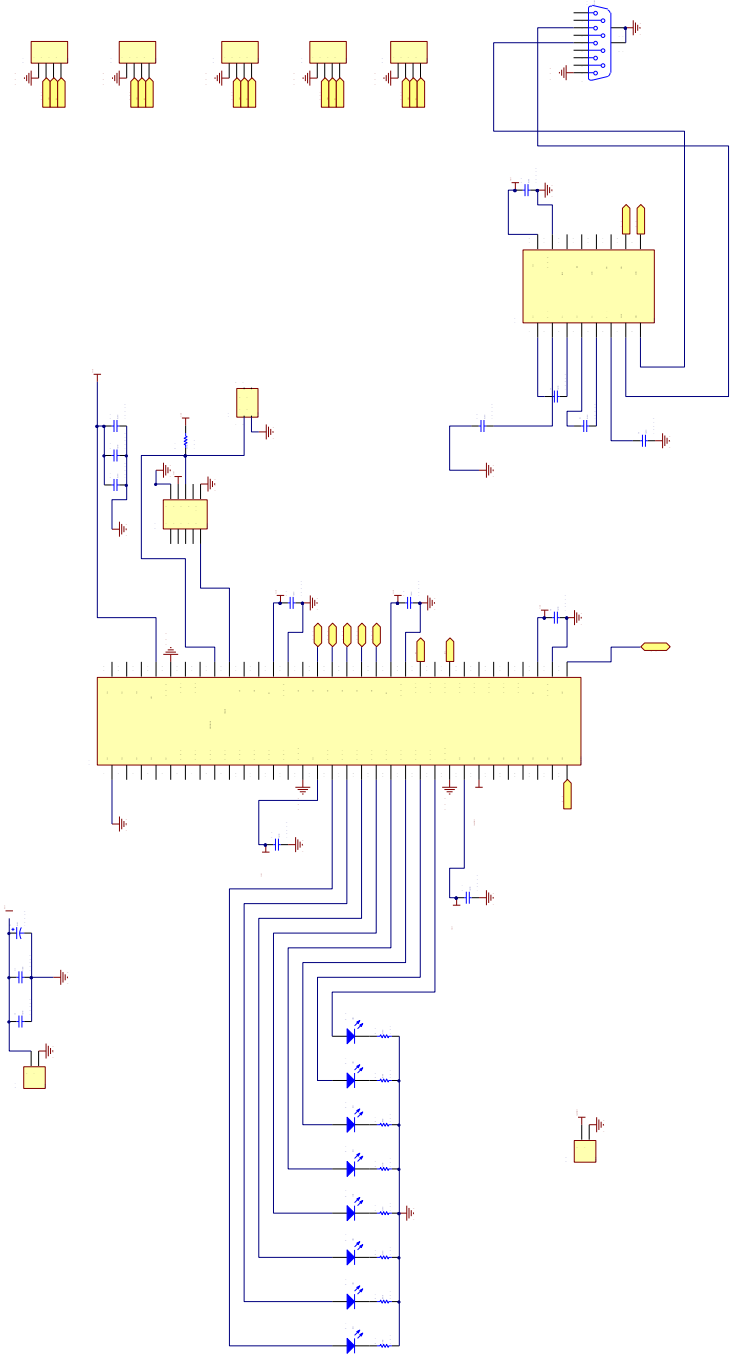

Figure C.3: Atmel Xmega 256B Schematic

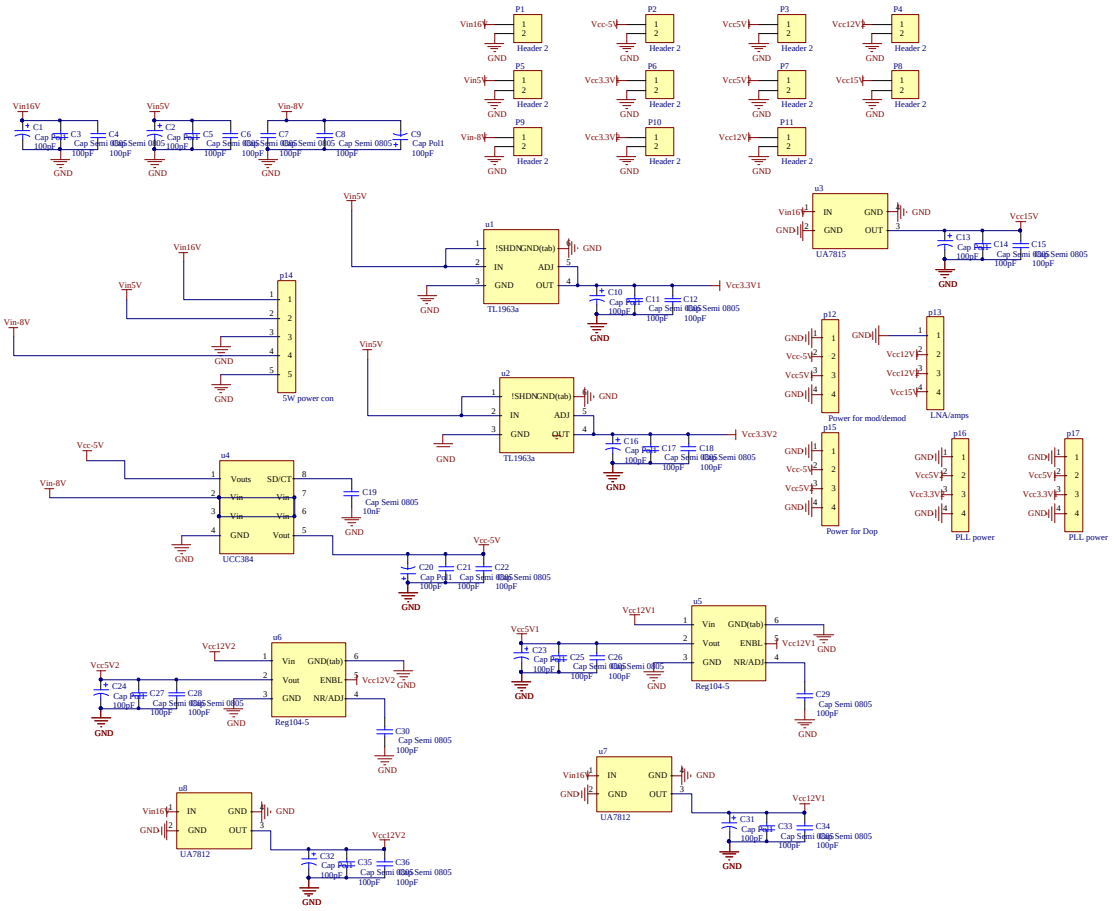

Figure C.4: Atmel Xmega 256B Schematic

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